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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION - PHASE II

BIPOLAR OP AMP STUDY

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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE II.

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BIPOLAR OP AMP STUDY.

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PREFACE

This document is one of eight task-oriented reports prepared under Contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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1. INTRODUCTION AND SUMMARY

The main thrust of Phase II of the Integrated Circuit Electromagnetic Susceptibility Investigation has been to develop a model of the effects to be expected in bipolar integrated circuits under RF stimulus. The approach has been to gather experimental data on the RF susceptibility of representative devices from the digital and linear subcategories, and to analyze the results to uncover the underlying physical phenomena. Prior to the work reported herein, an automated test system was developed [1] and used in studies of a 2-input NAND gate [2]. The 741 operational amplifier was chosen as a representative linear device since it is widely used by equipment designers.

The 741 operational amplifier was subjected to test stimuli at the frequencies of 0.22, 0.91, 3.0, 5.6, and 9.1 GHz in the automated test system. The 741 was observed to be more susceptible than the NAND gate to interference by three to four orders of magnitude. Catastrophic failure levels were similar to those for the NAND gate, but a degradation effect was found in the operational amplifier which was not observed in the NAND gate.

The interference mechanism in the 741 op amp is rectification of the RF stimulus in various device junctions. This was also the case in the NAND gate [2]. The 741 circuit is quite sensitive to very small currents which upset its normal balanced operation. Significant interference effects resulted from RF injection on any of the device's seven ports, but the two inputs and two offset null ports were particularly sensitive since less than 50 microwatts of absorbed power was capable of producing large output voltage changes.

The effects of the interfering RF signal can be modelled with a simple offset generator in the inverting input arm, thus permitting equipment designers to estimate overall circuit effects when the magnitude of the interference versus RF

drive level is known. At this time, it is still necessary to obtain experimentally the interference versus RF drive level information.

2. MEASURED RF EFFECTS IN THE 741 OPERATIONAL AMPLIFIER

The 741 operational amplifier was tested to determine its response to the injection of RF power. This response can be: interference, degradation, or catastrophic failure. Interference is the condition in which any device under RF stimulus exhibits abnormal behavior but which disappears when the stimulus is removed. Degradation is the condition in which a device, which has been exposed to an RF stimulus, exhibits a permanent abnormal behavior but is still operational to some degree. Catastrophic failure is the condition in which a device, which has been exposed to an RF stimulus, has failed completely and will not respond to any type of input.

In general, as the RF power level is increased, a device first experiences interference, then degradation, and finally failure.

2.1 Interference Effects - Abnormal behavior of the 741 operational parameters was observed under many varied conditions. This section describes the test conditions and the data obtained from the tests.

2.1.1 Interference Test Plan - The 741 is a monolithic bipolar operational amplifier on a single silicon chip. It has a high common mode rejection ratio, a large differential input voltage range, a high gain (50,000 minimum), a wide range of operating voltage ($\pm$18 volts), an offset voltage null capability, short circuit protection, and no requirement for external frequency compensation.

During interference testing the goal was to monitor all 741 parameters and test all combinations of frequency and RF injection port. Through this two-fold approach, the data base obtained would be as complete as possible. Also all tests were made on an actively-biased 741 operating as an inverting amplifier with a gain of ten. Therefore, the data obtained from the tests were realistic because the device was tested as an active device in a practical situation.

The following shows how the test conditions were set up:

1. Ten devices (to determine any device-to-device variations)
2. Seven entry ports per device (i.e., two inputs, two offset nulls, two power supply pins, and one output)
3. Five frequencies per port
4. Twenty RF power levels per frequency (including a zero run)
5. Sixteen circuit parameters per power level (seven dc currents, seven dc voltages, RF power absorbed, and RF calibration factor)

Therefore, 112,000 (10 x 7 x 5 x 20 x 16) data points were taken.

In order to minimize device-to-device variation and simplify analysis, all 741 devices tested were from one manufacturer and one date code. Through this precaution, internal circuitry variation was not a parameter.

The 741 chosen for test was in a ten-pin flatpack package. Figure 1 shows the external circuit used in testing the 741 as an inverting amplifier with a gain of 10. The seven pins shown in figure 1 became injection ports for RF power. The test fixture (shown in figure 2) was used and is described in reference 1. The five test frequencies were 0.22, 0.91, 3.0, 5.6, and 9.1 GHz. The power levels for each device covered the range from ten microwatts to one watt. The dc voltages and currents were measured at each port using the automated susceptibility measurement system (figure 3) which stored the data on magnetic tape. Complete block diagrams and explanations of the automated susceptibility measurement system may also be found in reference 1.

The microwave impedance of the 741 was checked for any irregularities in the RF properties of the device. Although the microwave impedance varies with port, frequency, and power level, the variation is not great enough to cause problems with the data. Also, the automated measurement system monitored RF data during each run so that any

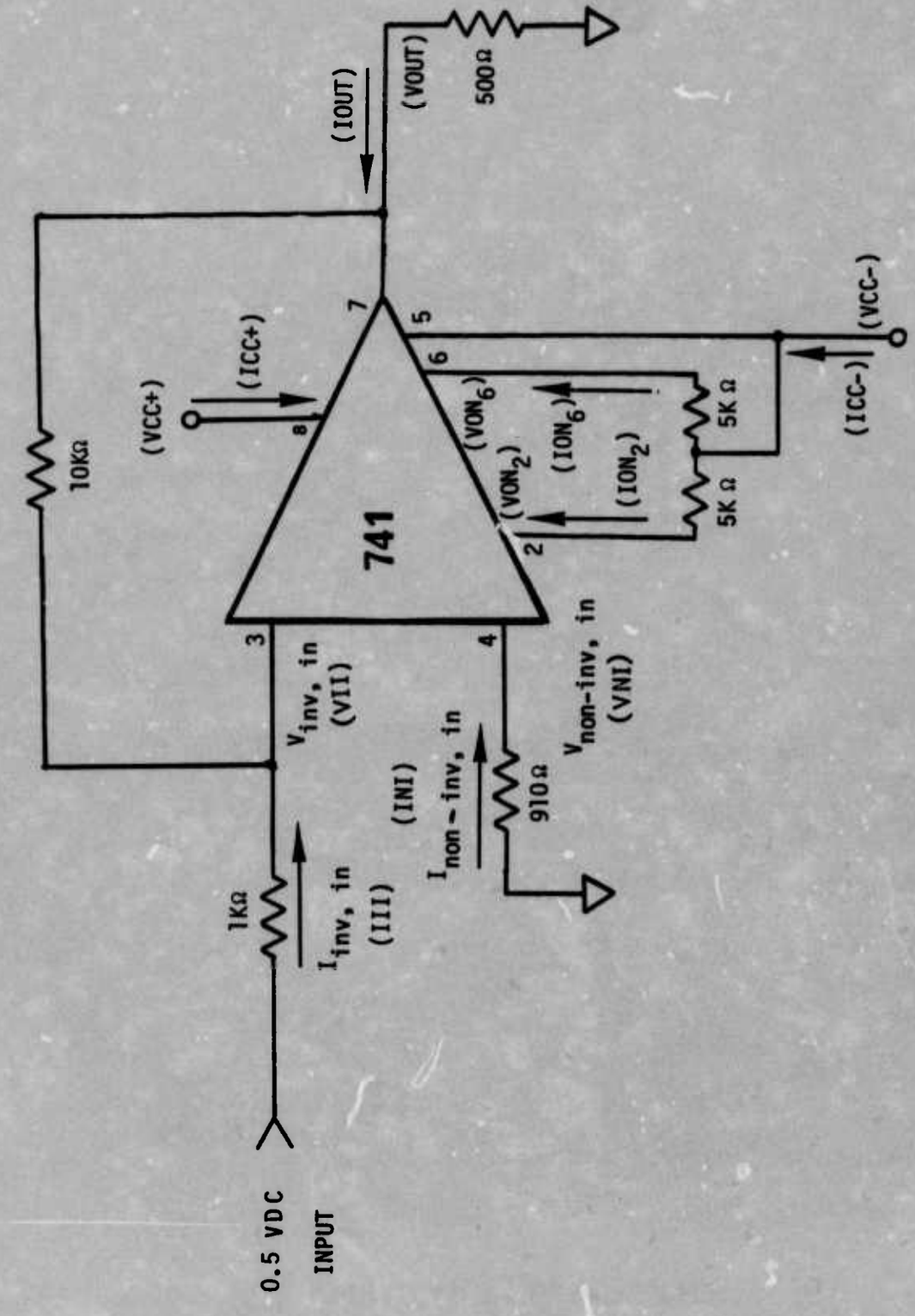

FIGURE 1 CIRCUIT USED FOR 741 SUSCEPTIBILITY MEASUREMENTS

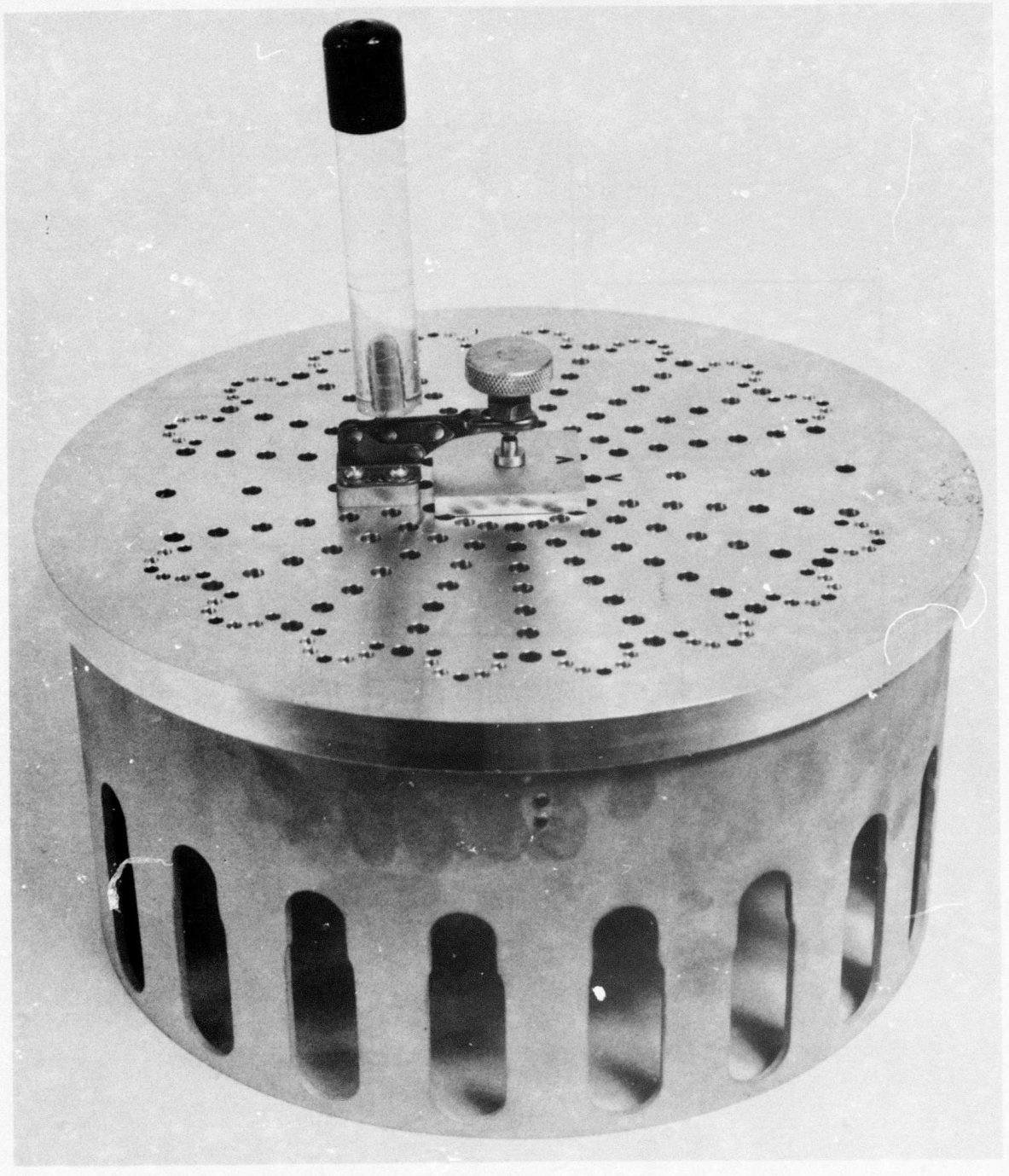

FIGURE 2 FLATPACK TEST FIXTURE

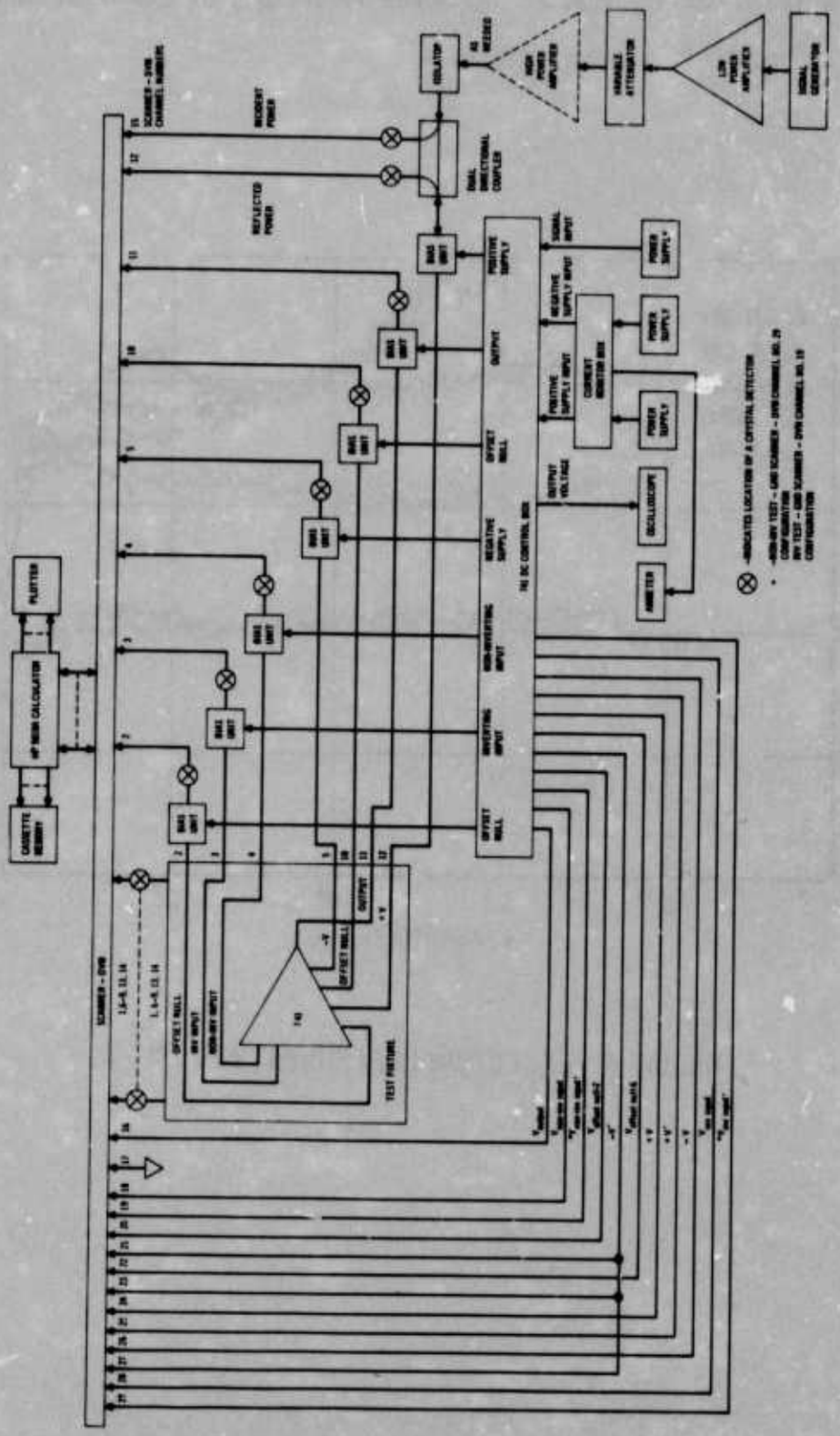

FIGURE 3 741 AUTOMATED SUSCEPTIBILITY MEASUREMENT SYSTEM

sudden or drastic changes in the RF properties would be known. The reflection coefficient, which shows the fraction of power reflected, of the inverting input as a function of power is shown in figure 4.

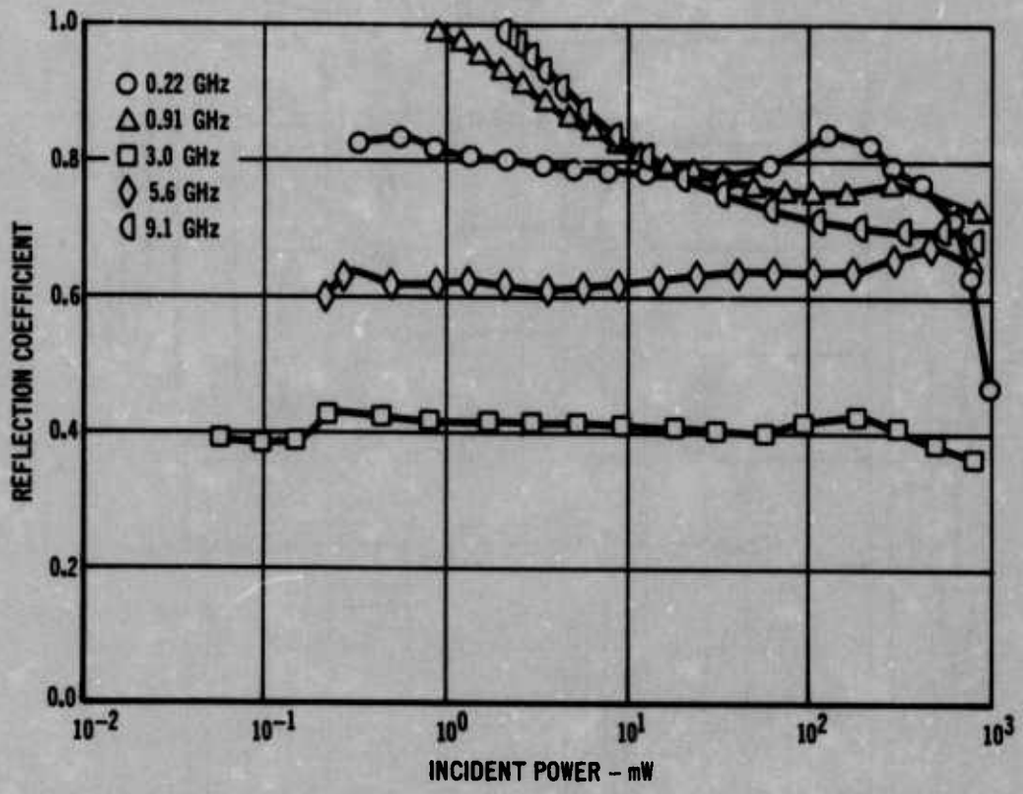

FIGURE 4 REFLECTION COEFFICIENT FOR 741

2.1.2 Interference Data - Table 1 is a sample listing of the data taken for one 741 during interference testing. These data were taken for all 350 devices (10 devices x 7 ports x 5 frequencies). It is relatively easy to scan these listings to determine which parameters are significantly affected by the RF stimulus. In general, the inverting input voltage and current and the output voltage and current (with corresponding supply current changes) are the best indicators of RF-induced effects.

The dc parameters of interest were plotted as a function of absorbed RF power to better show the trend. Each graph is a composite showing the data for all ten devices tested in the same configuration (as a check on data precision). For example, figure 5 shows the output voltage to be very sensitive to the RF power injected into offset null port 2 at 220 MHz. The complete collection of plots for V_{out} as a function of absorbed RF power for each combination of injection port and frequency are in Appendix A.

The plots of V_{out} vs $P_{absorbed}$ show that the output voltage varies greatly with RF power. Even at the lowest levels of RF power that can be measured with the automated measurement system and at the lower frequencies, V_{out} changes from its normal condition. Thus, in figure 5, the normal output voltage is -5.0 volts (indicated by the "X" in the margin) and the output voltage corresponding to the lowest value of absorbed power has changed more than one volt. Figure 5 also shows a strange phenomenon above 2 mW absorbed power. The output voltage switches and jumps from the vicinity of -8 volts to approximately +9 volts. This polarity switch is not an isolated case; rather, it appears on many of the V_{out} plots as shown in Appendix A.

TABLE 1 EXAMPLE OF 741 INTERFERENCE SUSCEPTIBILITY DATA

S/N = 120

P(mW)	C.F.(dB)	VOUT	IOUT	VNI	INI	VON2	ION2	VON6
-0.000	0.00	-4.896	9.79	-0.00	0.0000	-11.84	-0.0292	-11.84
0.093	9.42	-6.366	12.73	-0.00	0.0001	-11.80	-0.0368	-11.81
0.148	8.83	-6.521	13.04	-0.00	0.0001	-11.79	-0.0382	-11.80
0.191	9.86	-6.781	13.56	-0.00	0.0001	-11.79	-0.0390	-11.79
0.442	7.61	-7.340	14.68	-0.00	0.0001	-11.77	-0.0408	-11.78
0.600	7.70	-7.544	15.09	-0.00	0.0001	-11.77	-0.0422	-11.77
1.225	6.61	-7.542	15.08	-0.00	0.0001	-11.76	-0.0438	-11.77
1.310	7.01	-7.635	15.27	-0.00	0.0001	-11.75	-0.0454	-11.77
2.310	6.60	-7.435	14.87	-0.00	0.0001	-11.72	-0.0516	-11.78
3.675	7.27	9.647	-19.29	0.00	-0.0001	-11.82	-0.0352	-11.97
5.611	6.79	9.599	-19.20	0.00	-0.0002	-11.78	-0.0412	-11.97
9.093	6.13	9.349	-18.50	0.00	-0.0001	-11.62	-0.0758	-11.93
15.719	5.30	9.192	-18.38	0.00	-0.0002	-11.49	-0.1016	-11.89
23.724	4.87	9.151	-18.30	0.00	-0.0002	-11.41	-0.1174	-11.86
34.675	4.50	9.005	-18.01	0.00	-0.0001	-11.34	-0.1314	-11.86
53.610	4.22	8.748	-17.50	0.00	-0.0001	-11.24	-0.1526	-11.84
83.830	4.35	8.421	-16.84	0.00	-0.0001	-11.08	-0.1830	-11.82
124.458	4.40	7.907	-15.81	0.00	-0.0001	-10.97	-0.2010	-11.77
181.475	4.66	7.159	-14.20	0.00	-0.0001	-10.90	-0.2100	-11.67
214.113	4.72	6.663	-13.31	0.00	-0.0001	-10.87	-0.2262	-11.61

P(mW)	IOUT6	VCC+	ICC+	VCC-	ICC-	VII	III
-0.000	-0.0034	11.99	0.90	-11.87	-11.50	0.0007	0.4910
0.093	-0.0350	11.99	0.90	-11.83	-14.80	-0.1303	0.6239
0.148	-0.0364	11.99	0.90	-11.83	-15.10	-0.1404	0.6340
0.191	-0.0374	11.99	0.90	-11.82	-15.90	-0.1730	0.6666
0.442	-0.0392	11.99	0.90	-11.81	-16.60	-0.2090	0.7026
0.600	-0.0406	11.99	0.90	-11.80	-17.30	-0.2373	0.7308
1.225	-0.0406	11.99	0.90	-11.81	-17.30	-0.2351	0.7287
1.310	-0.0408	11.99	0.90	-11.80	-17.30	-0.2387	0.7323
2.310	-0.0402	11.99	0.90	-11.81	-17.00	-0.2266	0.7202
3.675	-0.0056	11.77	21.80	-11.99	-0.50	1.2940	-0.8005
5.611	-0.0056	11.78	21.60	-11.99	-0.50	1.3110	-0.8174
9.093	-0.0110	11.78	20.90	-11.99	-0.80	1.2980	-0.8044
15.719	-0.0226	11.78	20.80	-11.99	-0.80	1.2950	-0.8014
23.724	-0.0272	11.79	20.50	-11.99	-0.60	1.2870	-0.7934
34.675	-0.0282	11.79	20.40	-11.99	-0.60	1.2650	-0.7715
53.610	-0.0312	11.79	19.90	-11.99	-0.70	1.2430	-0.7494
83.830	-0.0360	11.80	19.40	-11.99	-0.90	1.2110	-0.7175
124.458	-0.0458	11.81	18.50	-11.99	-1.10	1.1620	-0.6685
181.475	-0.0652	11.82	17.10	-11.99	-1.50	1.0890	-0.5955
214.113	-0.0778	11.83	16.60	-11.98	-1.80	1.0560	-0.5624

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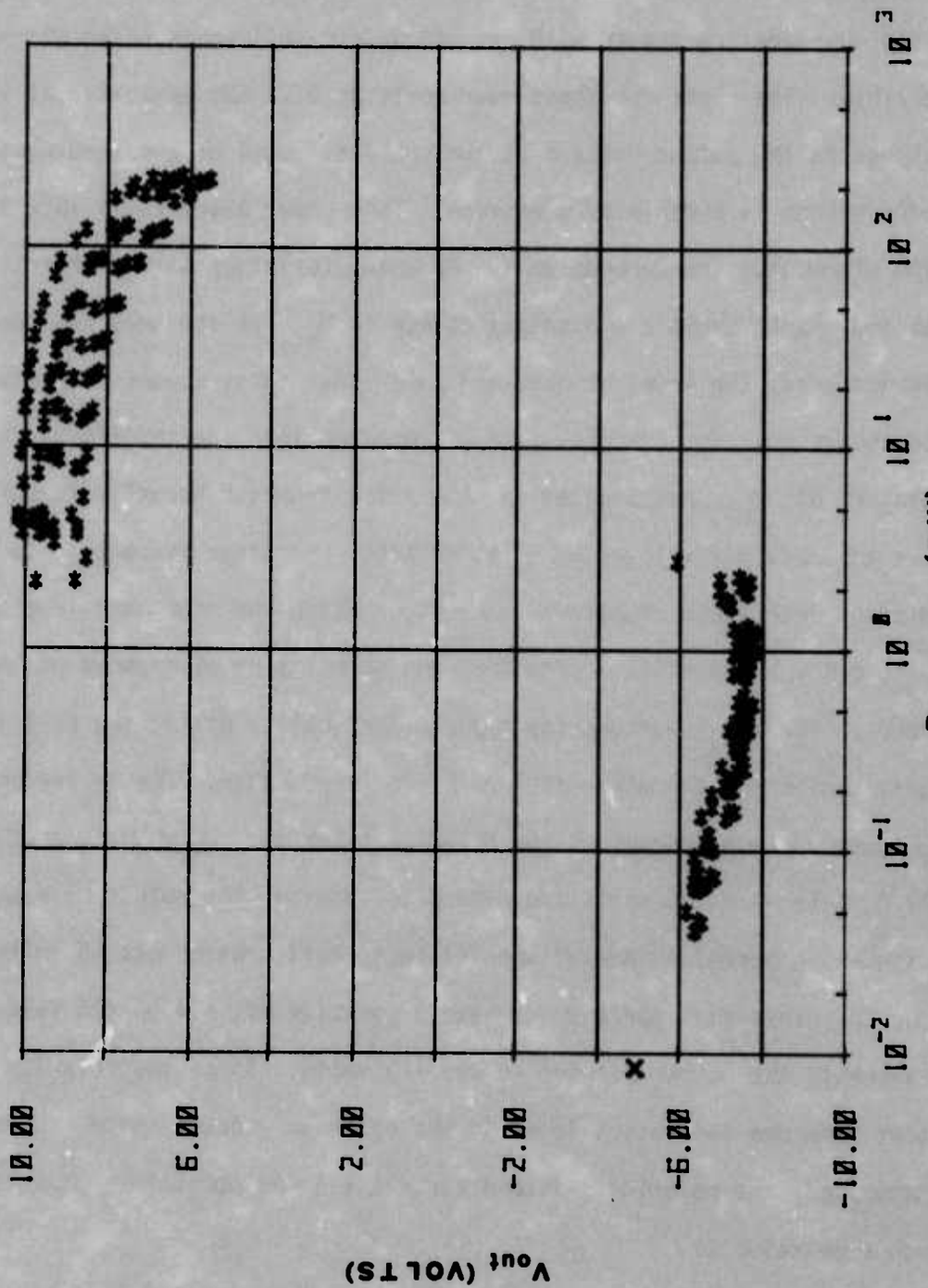

FIGURE 5 741 SUSCEPTIBILITY TO RF POWER INJECTED INTO OFFSET NULL 2 AT 0.22 GHz

For the 741, the factor which has been chosen to represent the observed effects is the change in output voltage (ΔV) for a given level of RF power absorbed in the device. From the plots in Appendix A, the most susceptible injection ports are the inverting and noninverting inputs with the two offset null ports being slightly less susceptible. The plots for these four ports at 0.22 GHz exhibited at least a one volt change in the output voltage at the smallest level of absorbed power that the automated system is capable of measuring. This power level falls into the range of 40 to 100 microwatts and depends on the RF characteristics of the injection port. Since these four ports exhibit a distinct change in V_{out} at the smallest power level that can be measured, the level of absorbed power that first causes a change in V_{out} can only be estimated. For example, with RF injected into the inverting input at 0.22 GHz (figure 6), V_{out} has dropped to -6.8 volts from its normal value of -5.0 volts for an absorbed power level of 60 microwatts. It seems reasonable to suppose that the minimum detectable signal would be at or below the microwatt level.

The V_{out} plots in Appendix A show that the polarity of ΔV depends on the injection port. For the inverting input and offset null 2 ports, the polarity of ΔV is negative while for the other five ports it is positive. The ΔV needed to bring V_{out} to saturation depends on the polarity. For the inverting input and offset null 2, only -4 to -5 volts are needed to saturate the output between -9 and -10 volts since the normal output of the 741 test configuration was -5 volts. However, for the other five ports which have a positive ΔV, +14 to +15 volts are needed to saturate the output between +9 and +10 volts. Since the polarity switch of the output from one saturation level to the other only occurs after the output has been saturated, the polarity switch occurs at a lower power level for the devices with a negative ΔV.

Figure 7 shows the V_{out} vs $P_{absorbed}$ plots with the RF injected into the non-inverting input. These plots show the frequency dependence of the susceptibility.

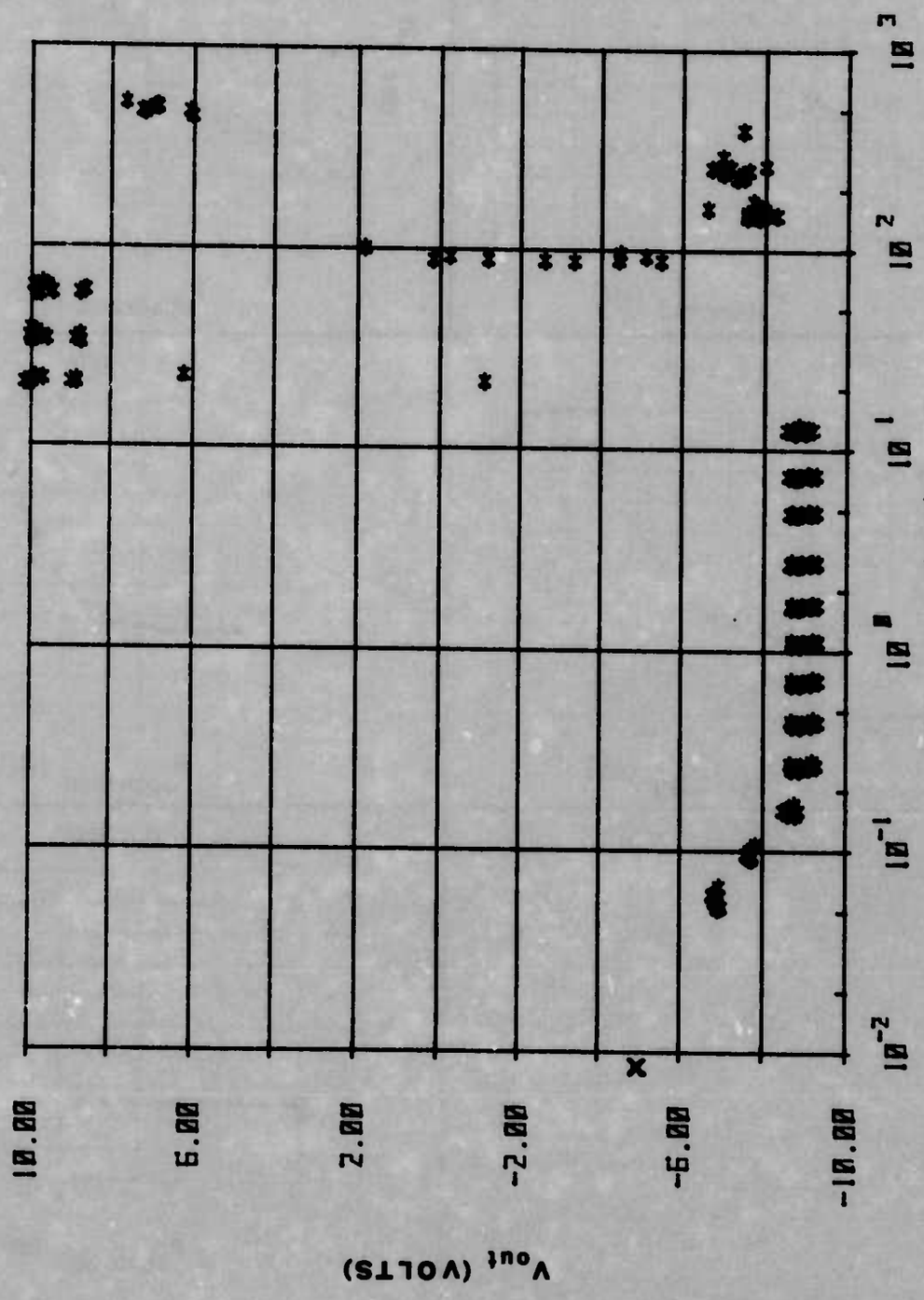

FIGURE 6 741 SUSCEPTIBILITY TO RF POWER INJECTED INTO THE INVERTING INPUT AT 0.22 GHz

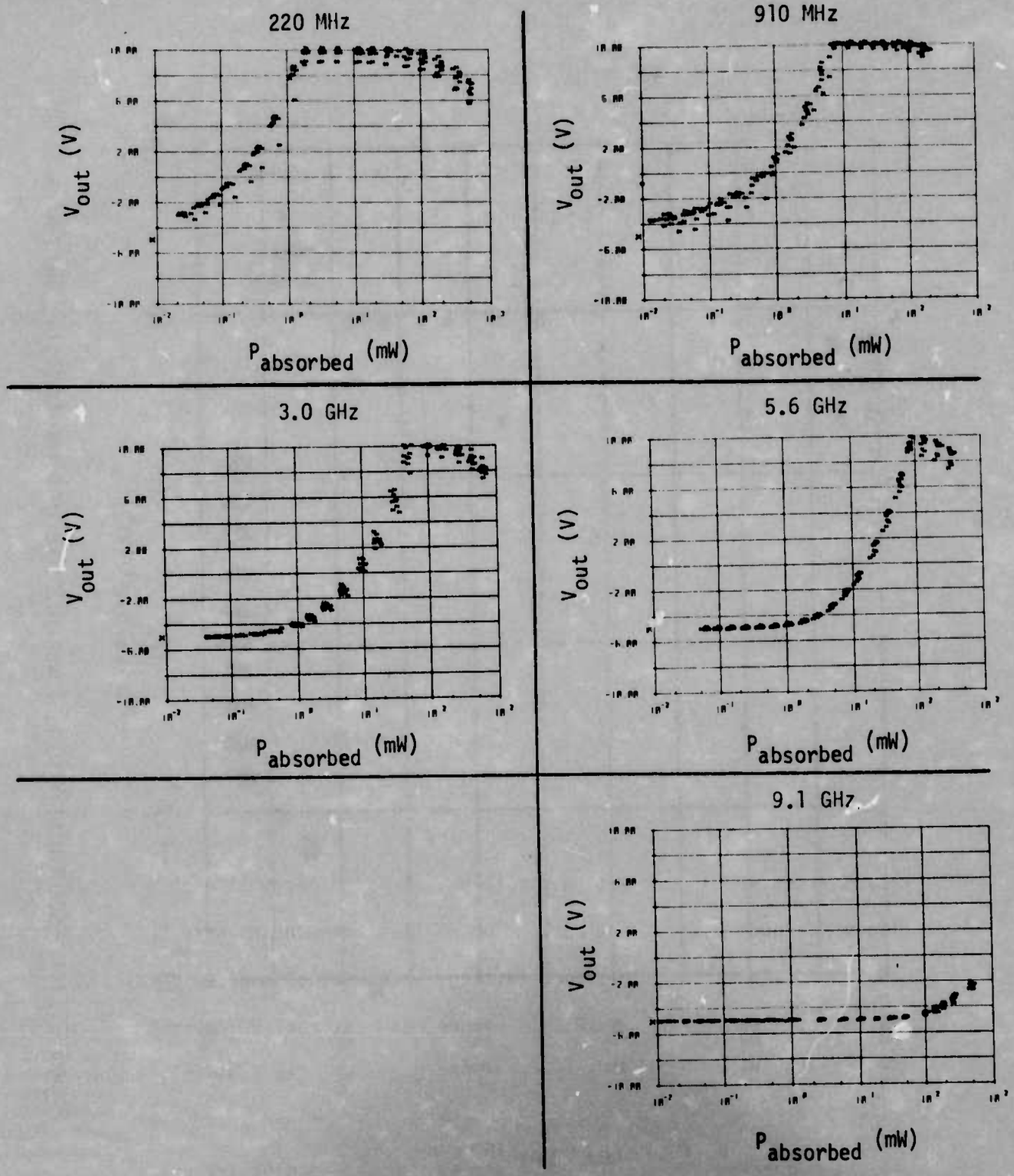

FIGURE 7 741 INTERFERENCE SUSCEPTIBILITY DATA WITH RF INJECTED INTO THE NON-INVERTING INPUT

As the frequency increases, the power level required to cause the same ΔV also increases such that, at 9.1 GHz, the output can not be saturated with the maximum allowable absorbed power ($\sim$500 mW). This is true for all injection ports on the 741. All ports are most susceptible at the lowest test frequency, and the susceptibility decreases as the frequency increases.

2.2 Degradation and Failure Effects - To determine the susceptibility of the 741 operational amplifier to a severe RF environment, high-power RF tests were conducted on the 741. During these tests, the 741 exhibited both permanent degradation in performance and catastrophic failure. Figure 8 is a photomicrograph of an undamaged 741 chip with the components labeled according to the schematic diagram in figure 9.

2.2.1 Degradation and Failure Test Plan - High-power, pulsed RF tests were conducted on the 741 operational amplifier in the same configuration as the interference tests. This test configuration, which was an inverting dc amplifier with a gain of ten, was shown in figure 1 with the normal input of 0.5 VDC. To determine the condition of the device after it was subjected to the RF pulse, the input to the 741 was changed to a 100 Hz sine wave with a peak-to-peak amplitude sufficient to drive the 741 into saturation. Figure 10 shows the output of an undamaged 741 as a function of the input voltage with the 100 Hz sine wave as the input.

Twenty devices were exposed to a single pulse of RF energy at each combination of frequency and input port. The RF test frequencies were 0.22, 0.91, 3.0, and 5.6 GHz. As with interference testing, each of the seven DC ports was used as an injection port for the RF. Therefore, 140 devices (20 devices x 7 ports) were tested at each frequency for a total of 560 devices. The available power was insufficient to fail the device at some combinations of frequency and port. In these cases, the energy in the pulse was increased by increasing the pulse width. The pulse was widened in steps: 0.5 msec, 1.0 msec, 2.0 msec, 5.0 msec, and 10 msec. If the device had not failed at 10 msec with the peak power available, it was declared nonsusceptible in that configuration.

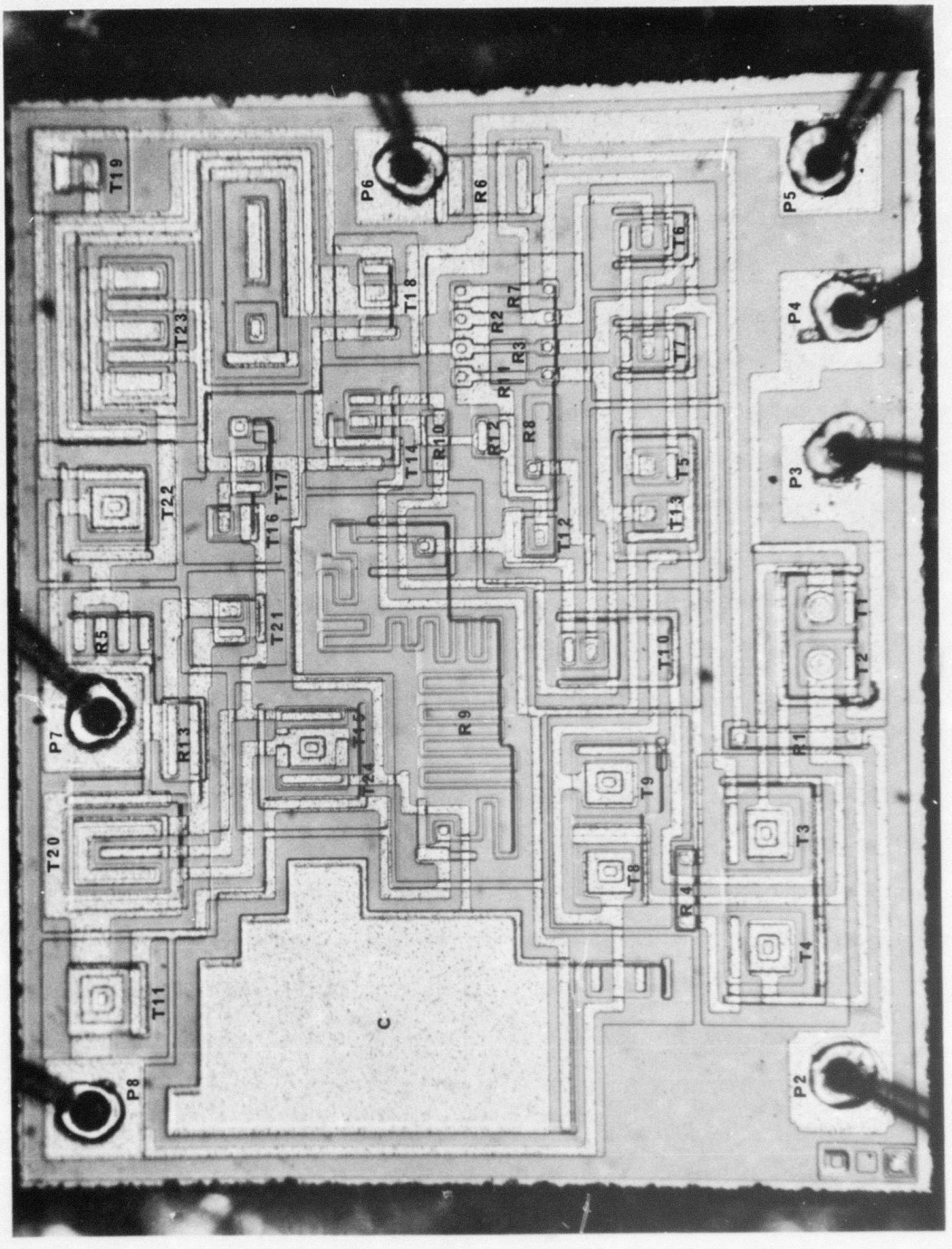

FIGURE 8 PHOTOMICROGRAPH OF 741 CHIP LAYOUT

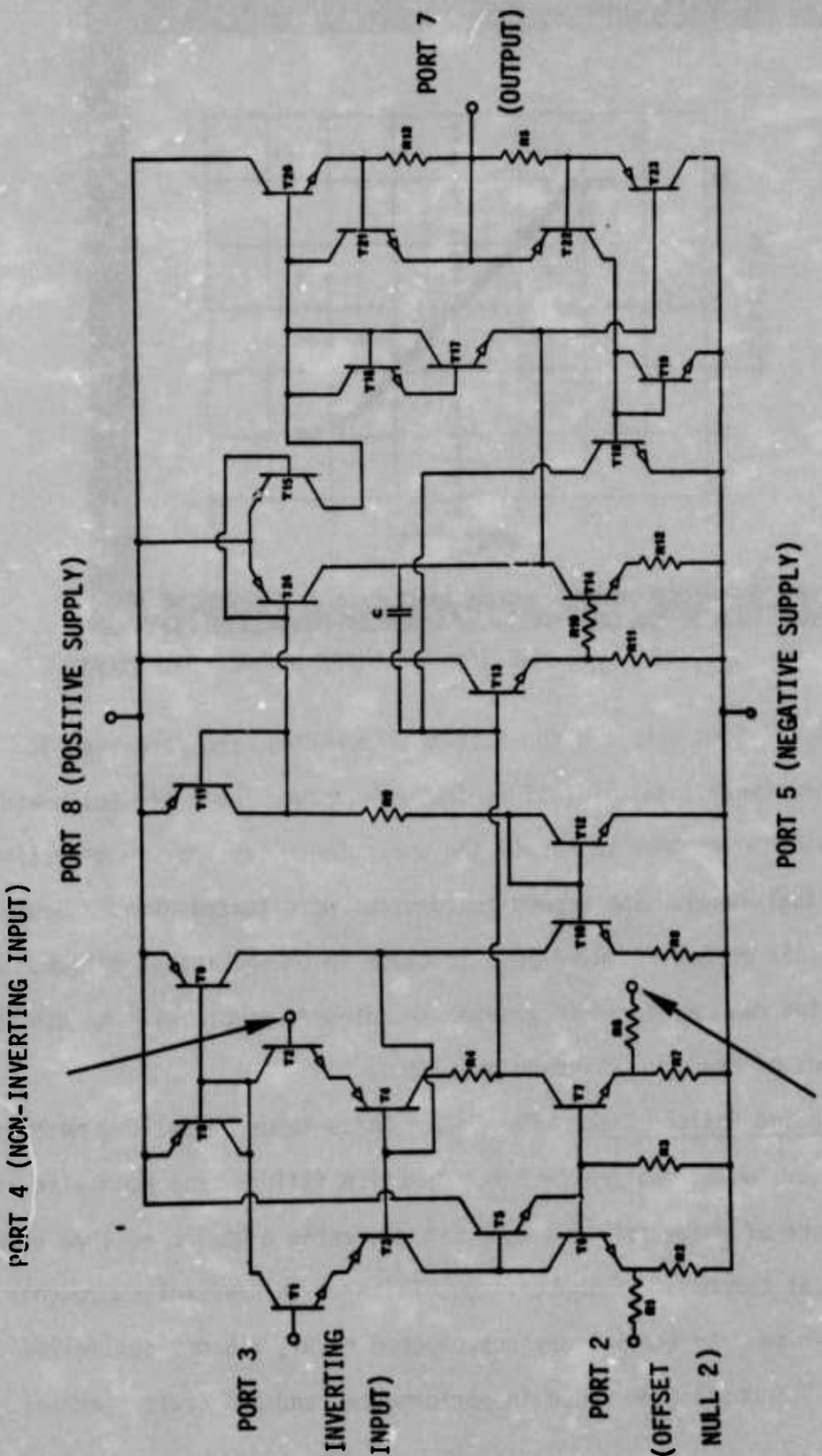

FIGURE 9 741 SCHEMATIC DIAGRAM

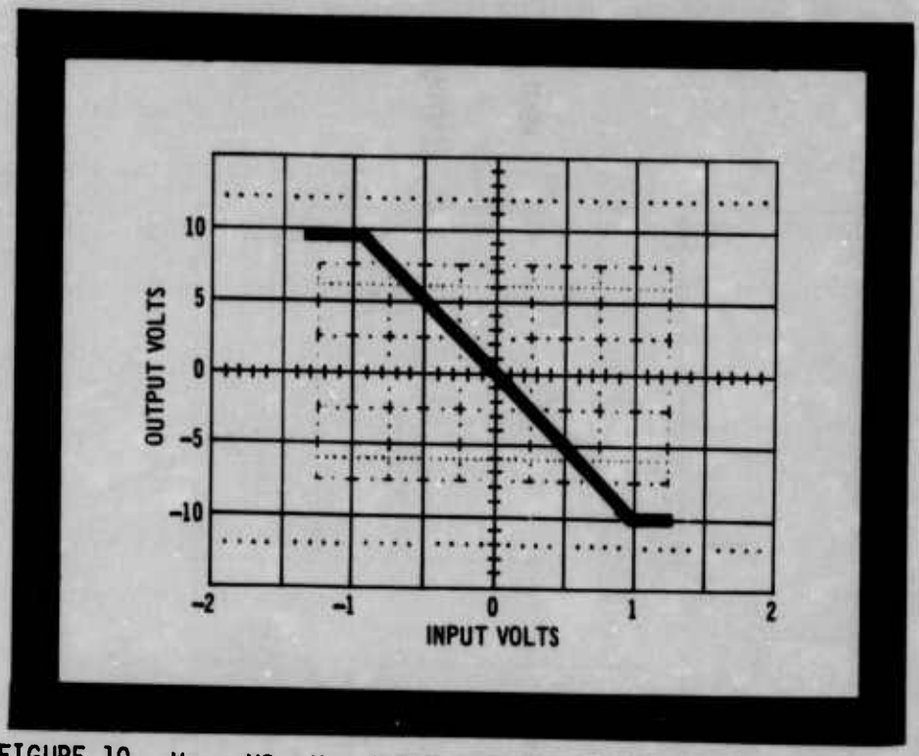

FIGURE 10 V_{out} VS V_{in} CURVE FOR 741 UNDER NORMAL CONDITIONS

Of the twenty devices allotted for each configuration, ten were used to determine the approximate level of failure including power level and pulse width. The other ten devices were used to verify the approximate level or to determine more accurately the actual level. The second ten devices were tested using a Bruceton-type test [2]. (This method was used just to close in on the actual failure level since the use of ten devices does not provide an adequate sample size to use the Bruceton statistics of mean and standard deviation).

2.2.2 Degradation and Failure Data - There were three types of failure mechanisms observed in the 741: metallization failure, junction failure, and bond wire failure. However, one or more of these failures does not guarantee a device failure unless it occurs in a vital component of the device. Failures in nonvital components will only cause degradation. Of the 560 devices exposed to RF, 215 devices failed catastrophically, 135 devices degraded in performance, and 210 devices exhibited no lasting effect.

2.2.2.1 Degradation - In the 741, the degradation observed was an offset to the normal output-vs-input curve (figure 10). Figure 11 shows this offset in the output-vs-input curve for a degraded device. This curve indicates that the device still functions as an amplifier at least over a restricted range. In fact, capacitor-coupled applications may not be bothered by this effect (except for reliability factors). With some input ports, such as the offset null ports, it was easy to obtain degraded devices. However, it was impossible to degrade a device using the output port as the RF injection port.

All three types of failure mechanisms were capable of causing degradation in the 741. However, the damage from any mechanism could be classified into one of two categories: 1) changes in the internal offset null circuitry, or 2) changes to one of the two input transistors. If the dc path to either offset null was broken by metallization or bond wire failures, then the device degraded rather than failed.

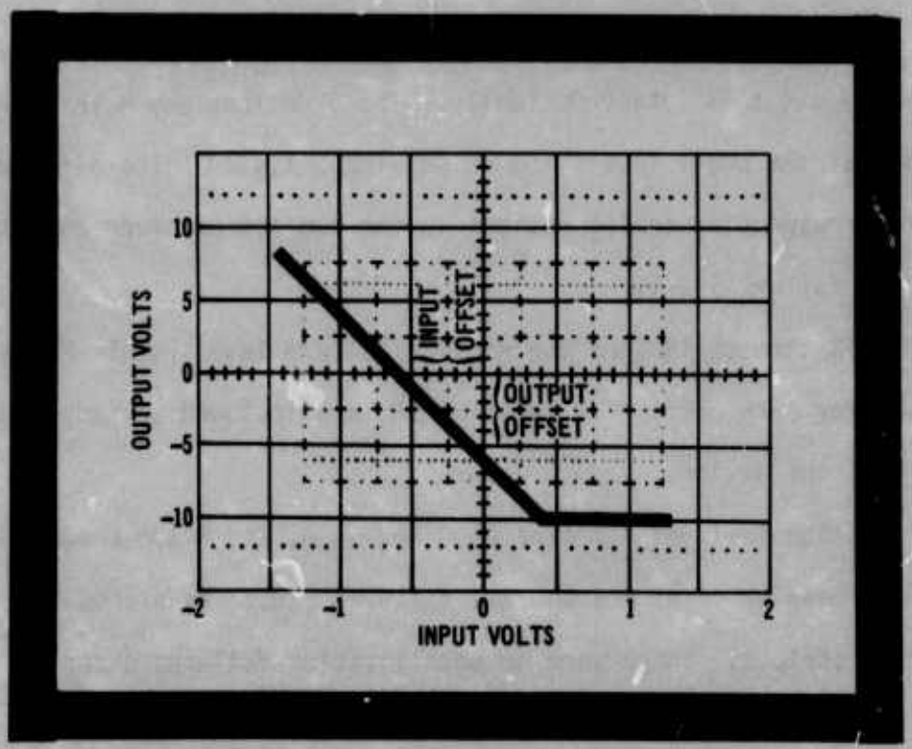

FIGURE 11 V_{out} VS V_{in} CURVE FOR DEGRADED 741

If the emitter-base junction of either input transistor was shorted by melted metallization flow across the junction, then the device would be at least degraded. This condition was often accompanied by failure of a vital component somewhere else on the chip.

2.2.2.2 Catastrophic Failure - All three failure mechanisms were capable of causing catastrophic failure in the 741. Of the 215 failures, 79 were metallization failures, 65 were junction failures, 67 were bond wire failures, and 4 were of undetermined cause. Table 2 shows the types of failures vs RF frequency and injection port. The power levels listed in Table 2 are minimum values at which a failure occurred for each combination of frequency and port, and the pulse width listed is the one corresponding to the power level given.

There exists, in the failure data, a device-to-device variation such that some devices did not fail at the minimum level given in table 2. Table 3 shows the maximum no-fail condition observed for the devices under test. This condition, expressed in power and pulse width, is the maximum observed amount at which at least one device did not fail catastrophically. These devices may have degraded but they did not fail at the power levels and pulse widths listed. The difference in the levels for corresponding configurations in the two tables gives an estimate of the spread of the failure levels.

Figures 12 through 18 show the minimum failure levels(table 2) as a function of frequency for each port. The pulse widths are included to indicate the energy needed to fail the device.

Metallization failures for pins 2, 3, 4, 5, 6, and 8 are shown in figures 19 through 24. These failures are thermal failures caused by excessive current in the metallization stripes. There were no metallization failures observed on pin 7, the 741 output pin.

TABLE 2 741 FAILURE MODES AND LEVELS

PIN / FREQ	NON-INVERTING INPUT	INVERTING INPUT	OFFSET NULL 2	OFFSET NULL 6	$+V_{cc}$	$-V_{cc}$	OUTPUT
220 MHz	3 metal 6 junction 0 bond (4.6 @ .5)	2 metal 7 junction 0 bond (4.4 @ .5)	9 metal 0 junction 0 bond (3.4 @ .5)	no failures (>64.7 @ 10)	0 metal 10 junction 0 bond (15.5 @ .5)	8 metal 0 junction 0 bond (12.5 @ .5)	0 metal 3 junction 0 bond (33 @ .5)
910 MHz	1 metal 7 junction 0 bond (1.75 @ .5)	0 metal 9 junction 0 bond (1.75 @ .5)	8 metal 0 junction 0 bond (8.8 @ .5)	no failures (>26.6 @ 10)	no failures (>30 @ 10)	no failures (>23.7 @ 10)	0 metal 0 junction 1 bond (23.6 @ 10)
3.0 GHz	8 metal 6 junction 0 bond (2 @ .5)	4 metal 10 junction 0 bond (2.4 @ .5)	9 metal 0 junction 0 bond (6.3 @ .5)	6 metal 0 junction 5 bond (41 @ 2 65 @ 1)	3 metal 6 junction 0 bond (15 @ .5)	10 metal 0 junction 0 bond (4.9 @ .5)	0 metal 1 junction 7 bond (13 @ 2)
5.6 GHz	0 metal 0 junction 13 bond (4 @ 5)	0 metal 0 junction 11 bond (6.9 @ 10)	8 metal 0 junction 0 bond (48 @ 1)	0 metal 0 junction 2 bond (37 @ 10)	0 metal 0 junction 10 bond (9.8 @ 5)	0 metal 0 junction 9 bond (6.2 @ 10)	0 metal 0 junction 9 bond (7.7 @ 10)

x metal = No. metalization failures
x junction = No. junction failures
x bond = No. bond wire failures
(x watts (min) @ y milliseconds)

TABLE 3 741 MAXIMUM NO FAIL CONDITION (POWER IN WATTS, PULSE WIDTH IN msec)

PIN FUNCTION / FREQUENCY	NON-INVERT INPUT 4	INVERTING INPUT 3	OFFSET NULL 2	OFFSET NULL 6	$+V_{cc}$ 5	$-V_{cc}$ 8	OUTPUT 7
220 MHz	5.92 @ .5	5.45 @ .5	5.37 @ .5	> 64.7 @ 10.	20 @ .5	19.5 @ .5	32.1 @ 2.
910 MHz	3.5 @ .5	2.74 @ .5	17.7 @ .5	> 26.6 @ 10	23.7 @ 10.	30. @ 10.	23.6 @ 10.
3.0 GHz	6.27 @ .5	2.95 @ .5	25.2 @ .5	65.5 @ 2.	6.14 @ .5	23.9 @ .5	25.9 @ 2.
5.6 GHz	15.7 @ .5	10.9 @ 10.	48.6 @ 1.	> 37.3 @ 10.	12.4 @ 10	7.87 @ 5.	9.75 @ 10.

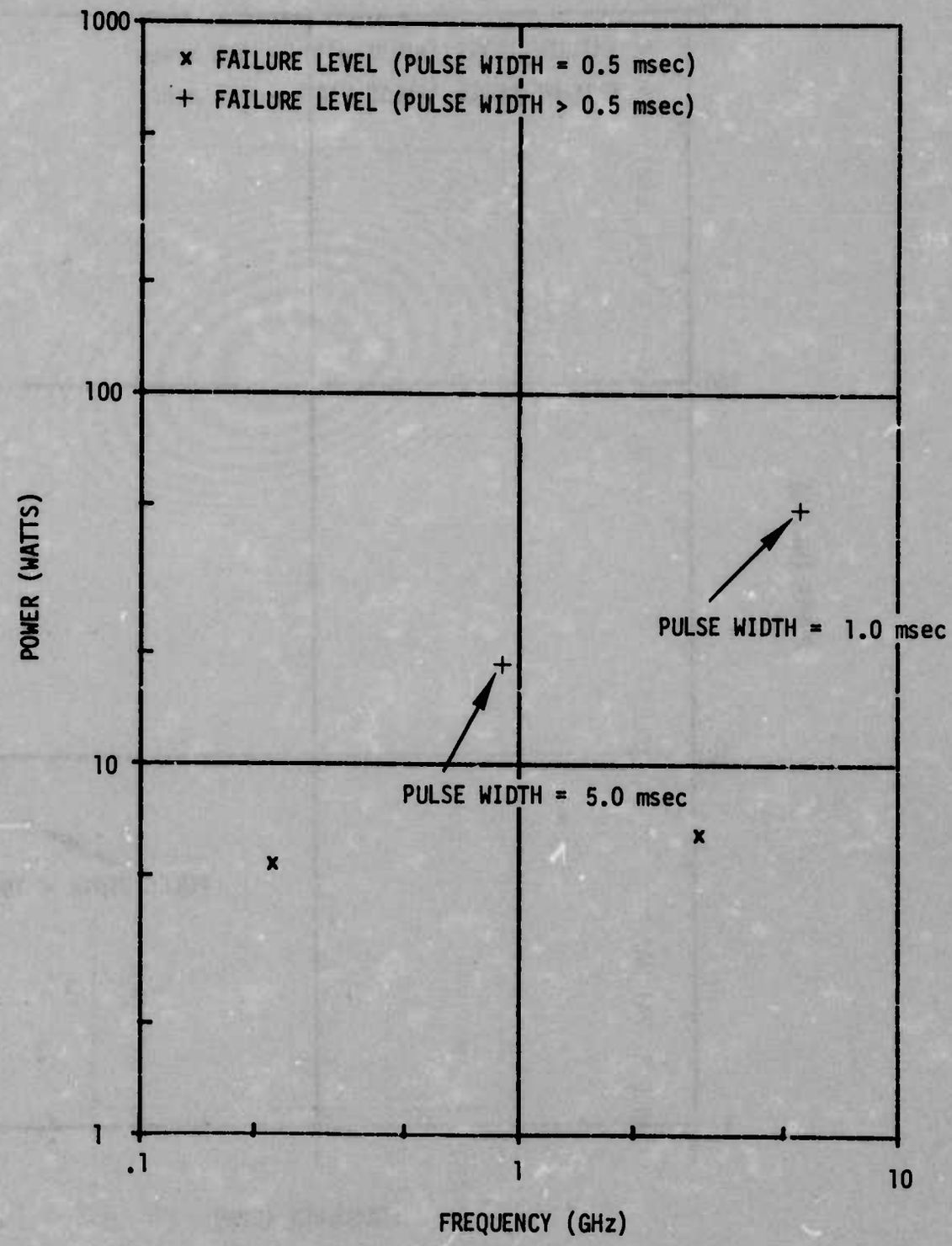

FIGURE 12 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT OFFSET NULL 2 PORT

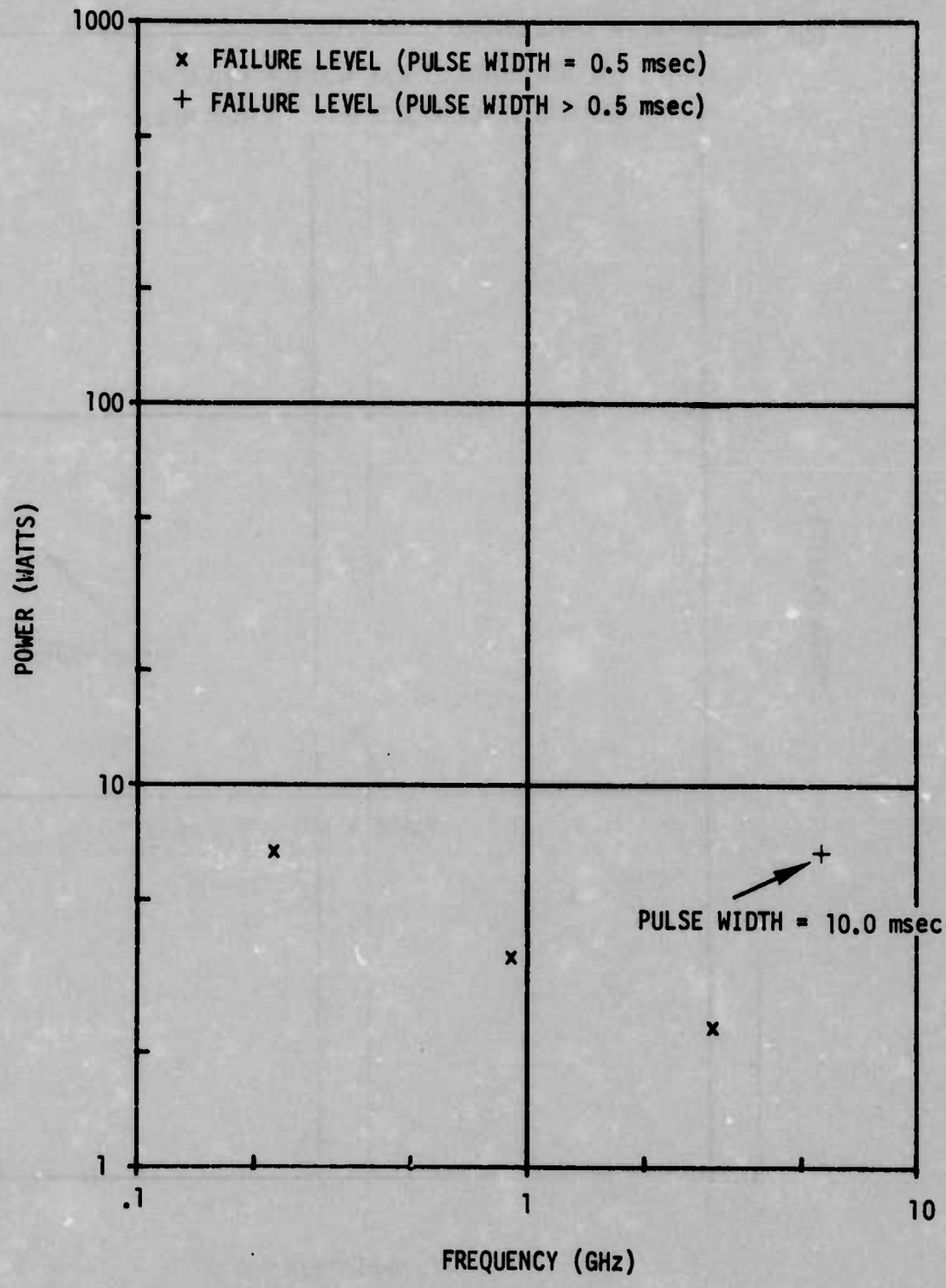

FIGURE 13 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE INVERTING INPUT PORT

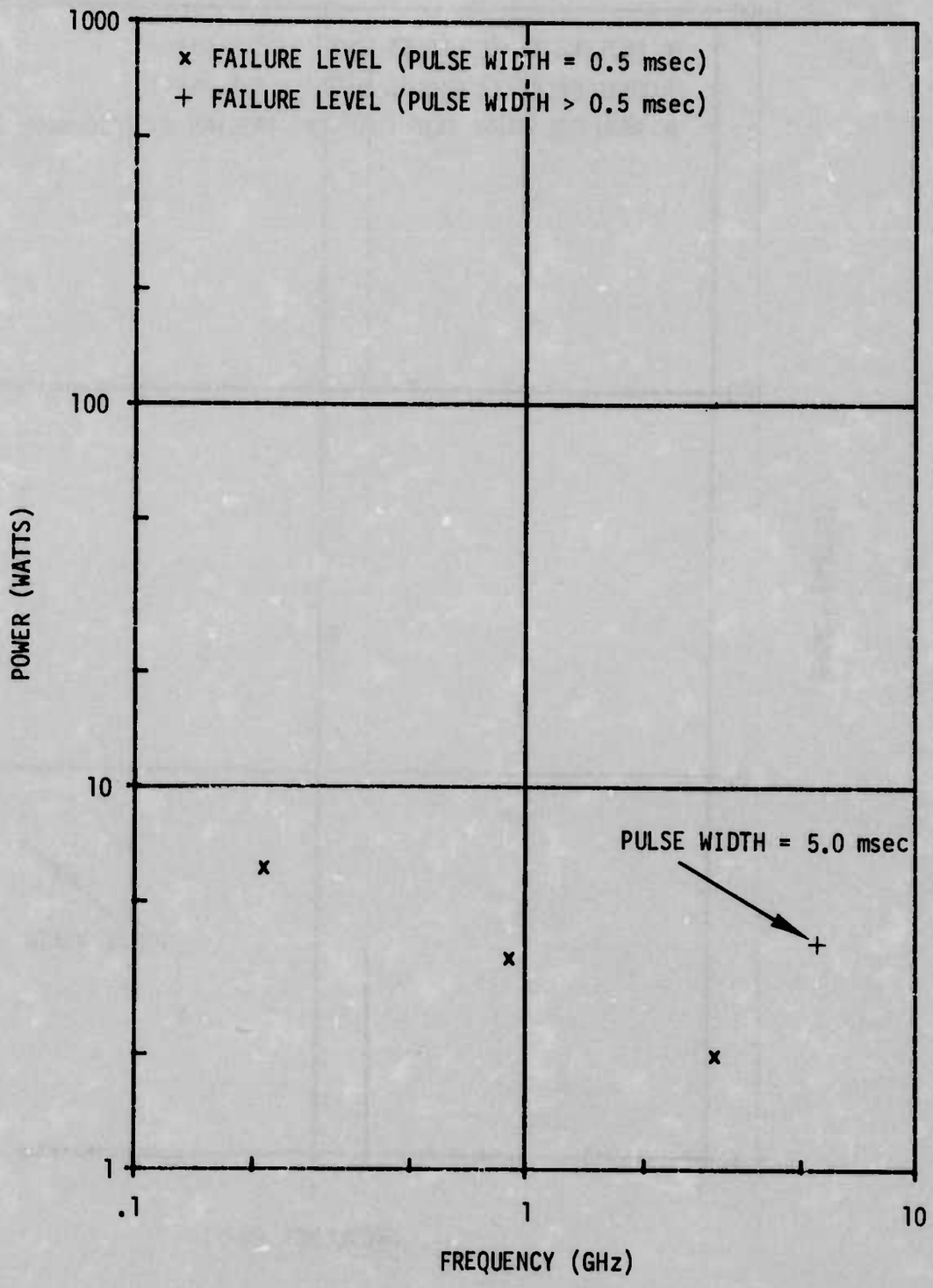

FIGURE 14 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE NON-INVERTING INPUT PORT

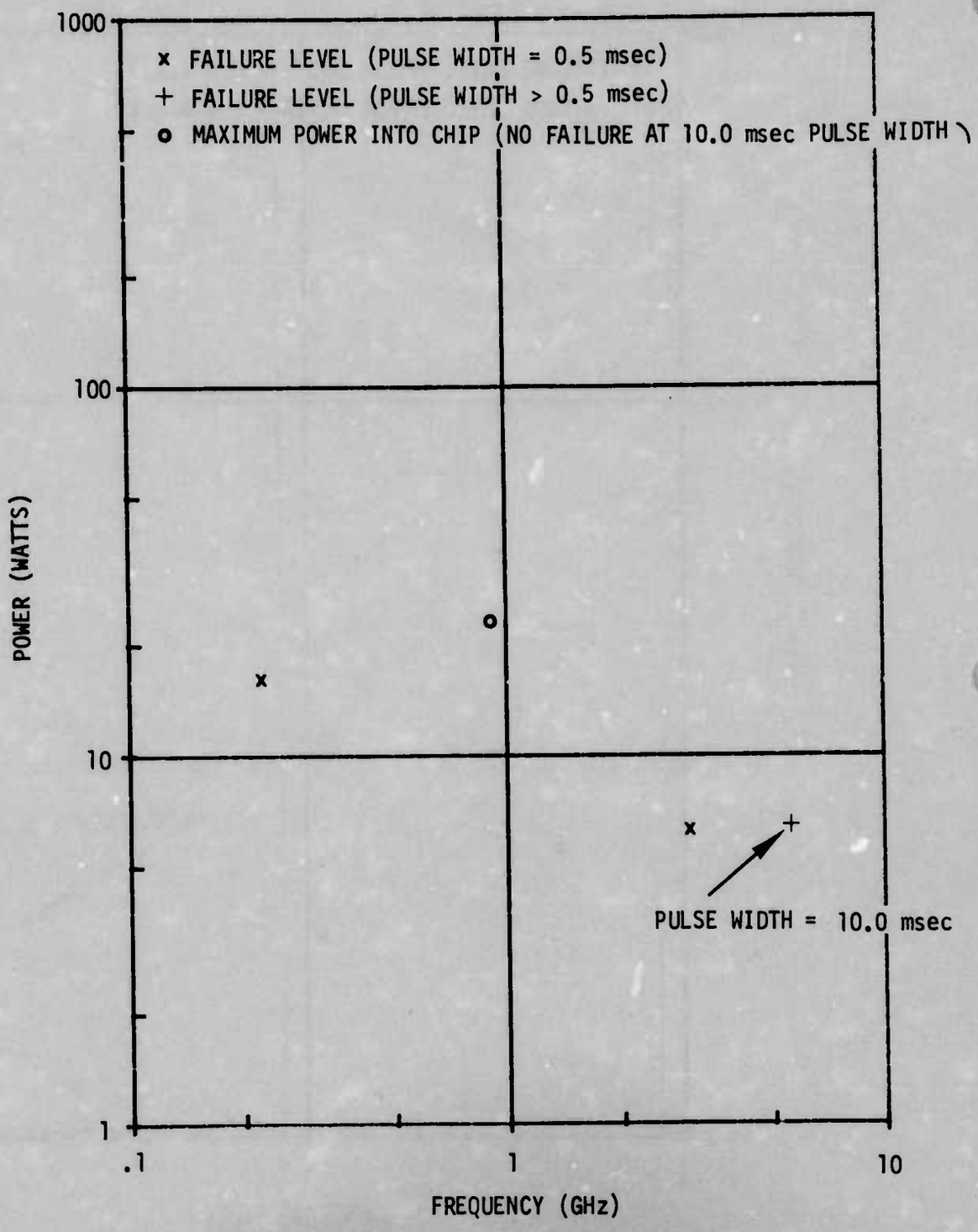

FIGURE 15 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE NEGATIVE SUPPLY PORT

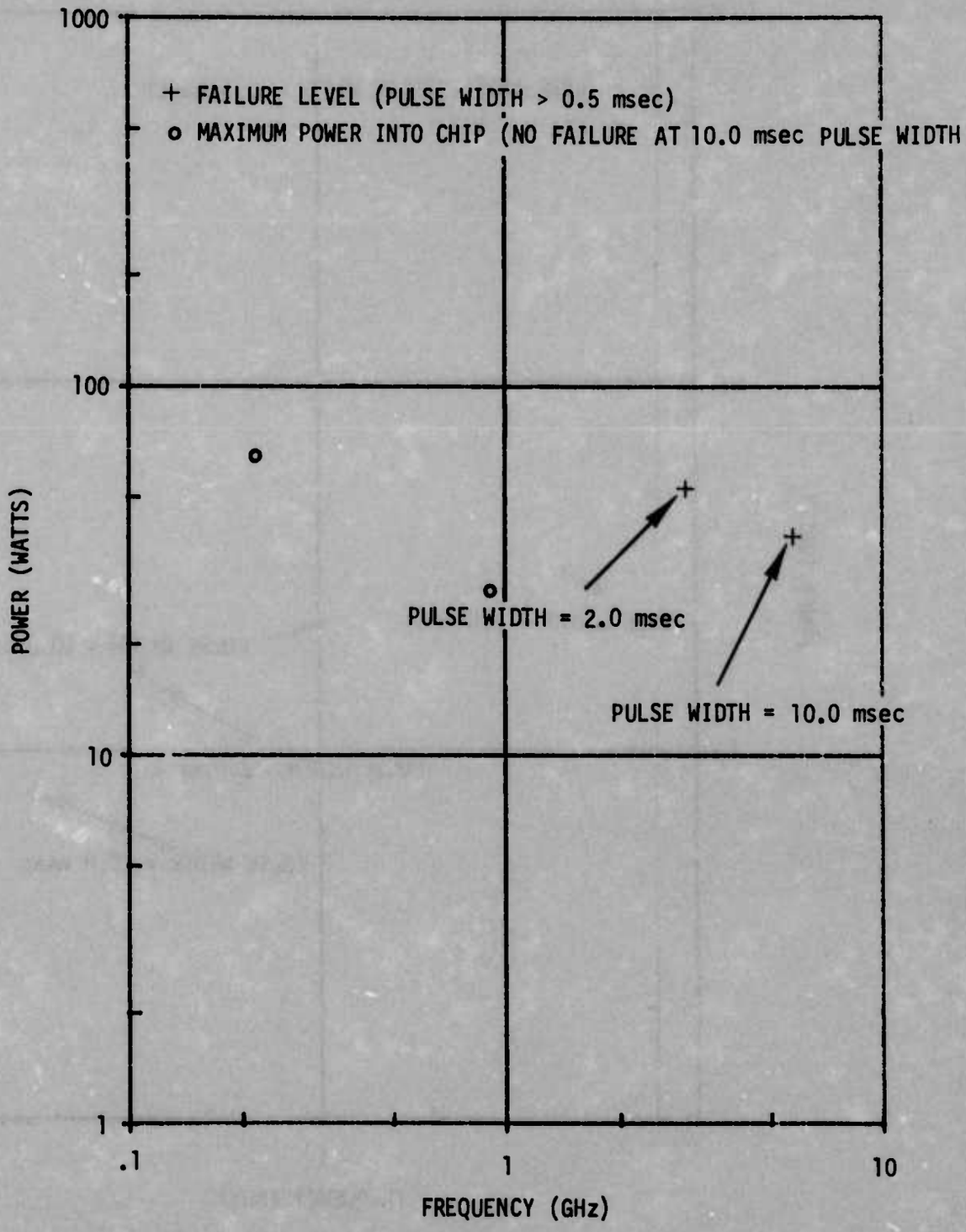

FIGURE 16 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT OFFSET NULL 6 PORT

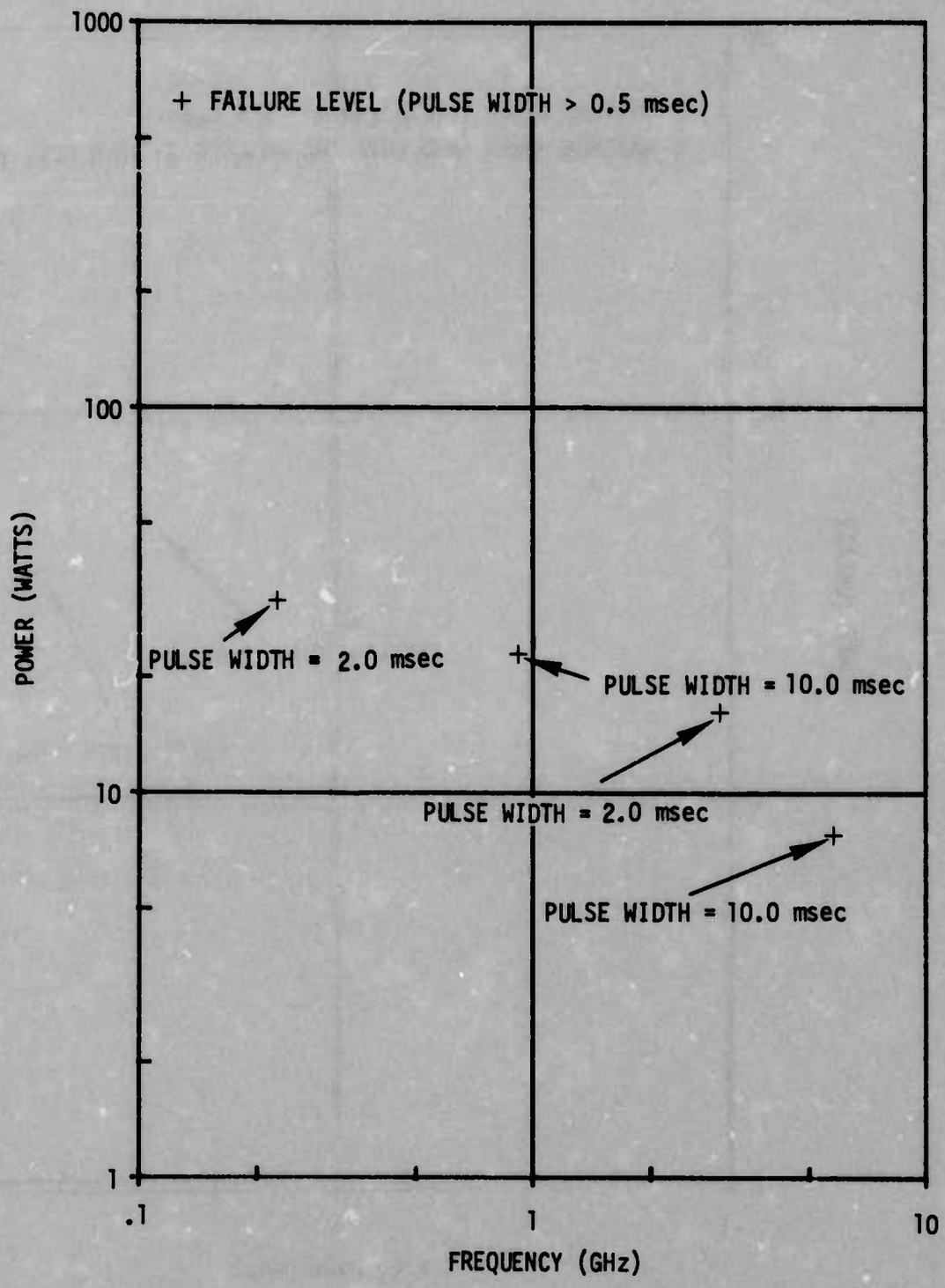

FIGURE 17 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE OUTPUT PORT

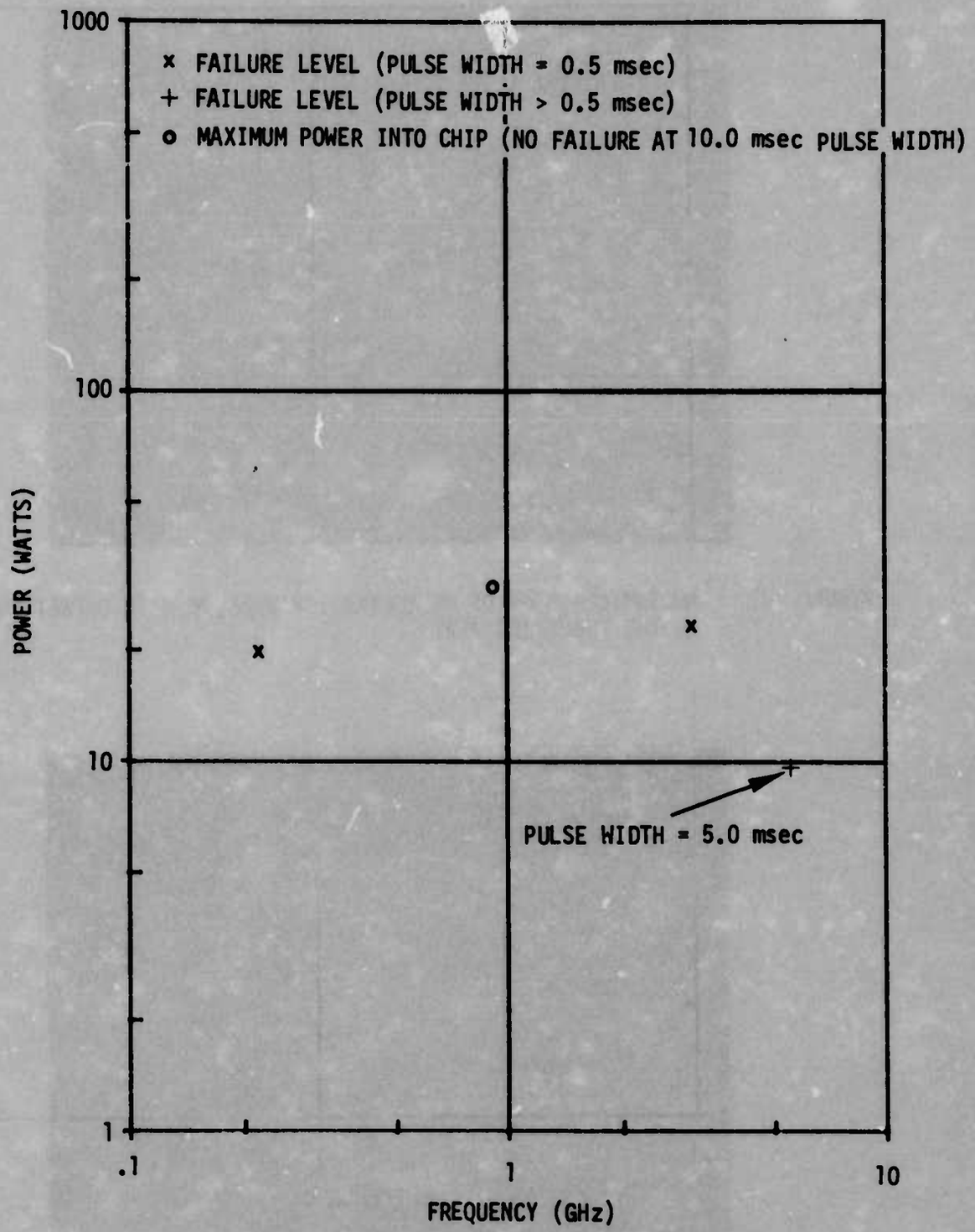

FIGURE 18 MINIMUM ABSORBED RF POWER REQUIRED TO CAUSE CATASTROPHIC FAILURE AT THE POSITIVE SUPPLY PORT

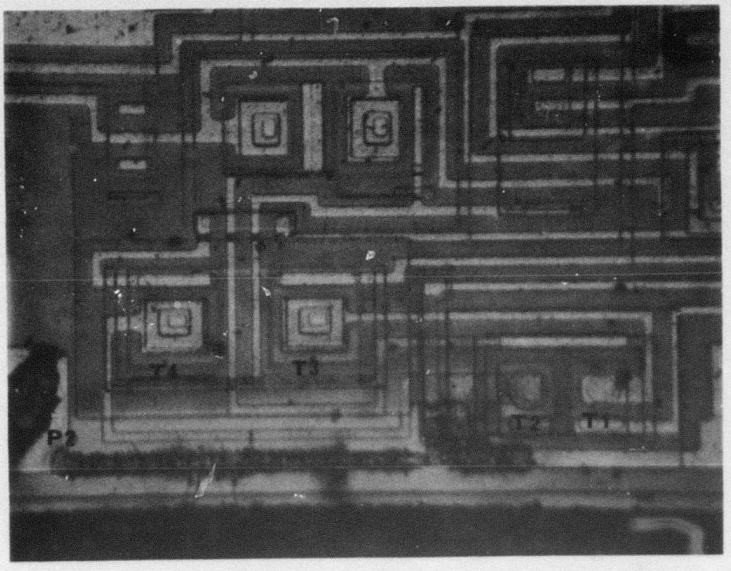

FIGURE 19 PHOTOMICROGRAPH OF METALLIZATION FAILURE WITH OFFSET NULL PORT 2 AS THE INJECTION PORT

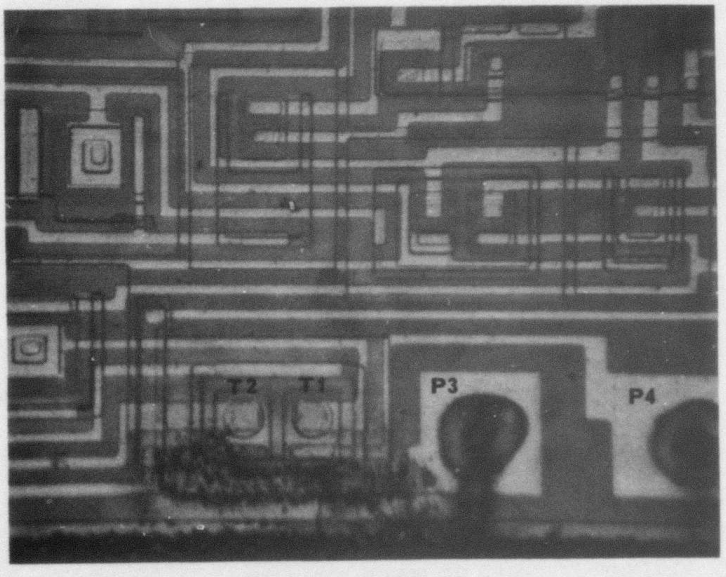

FIGURE 20 PHOTOMICROGRAPH OF METALLIZATION FAILURE WITH THE INVERTING INPUT AS THE INJECTION PORT

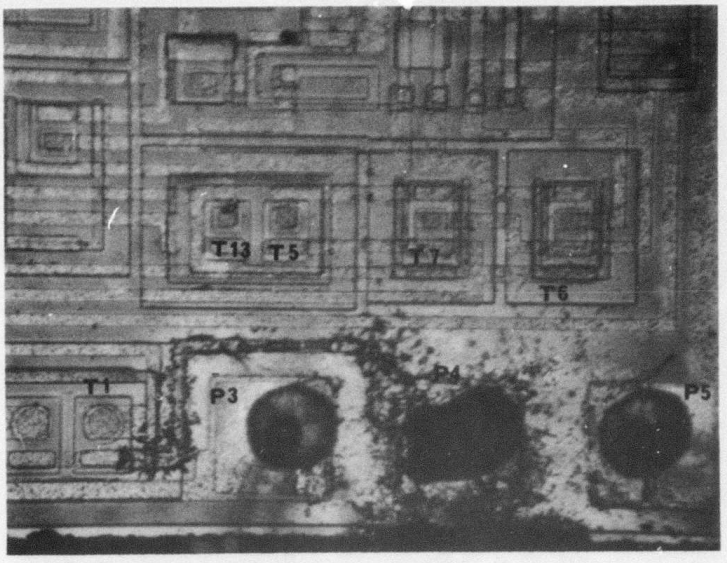

FIGURE 21 PHOTOMICROGRAPH OF METALLIZATION FAILURE WITH THE NON-INVERTING INPUT AS THE INJECTION PORT

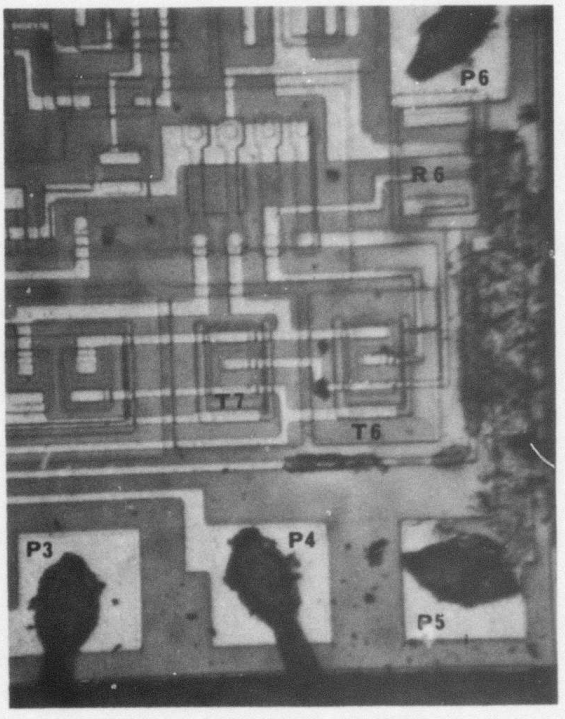

FIGURE 22 PHOTOMICROGRAPH OF METALLIZATION FAILURE WITH THE NEGATIVE SUPPLY AS THE INJECTION PORT

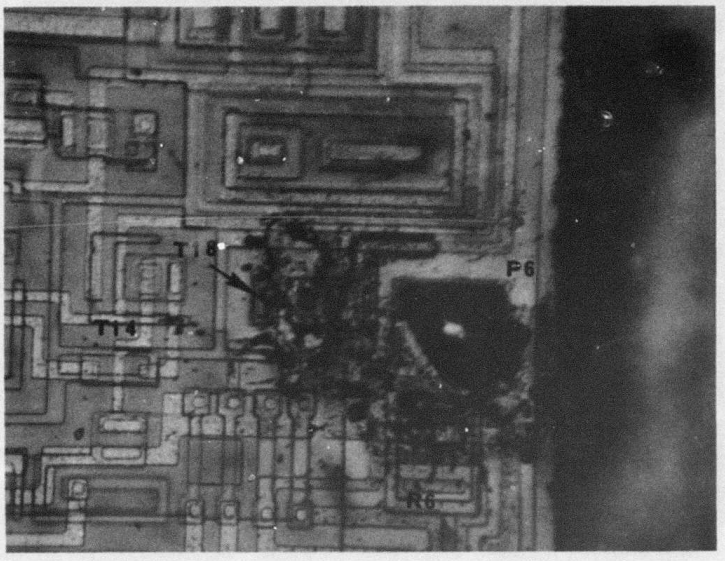

FIGURE 23 PHOTOMICROGRAPH OF METALLIZATION FAILURE WITH OFFSET NULL 6 AS THE INJECTION PORT

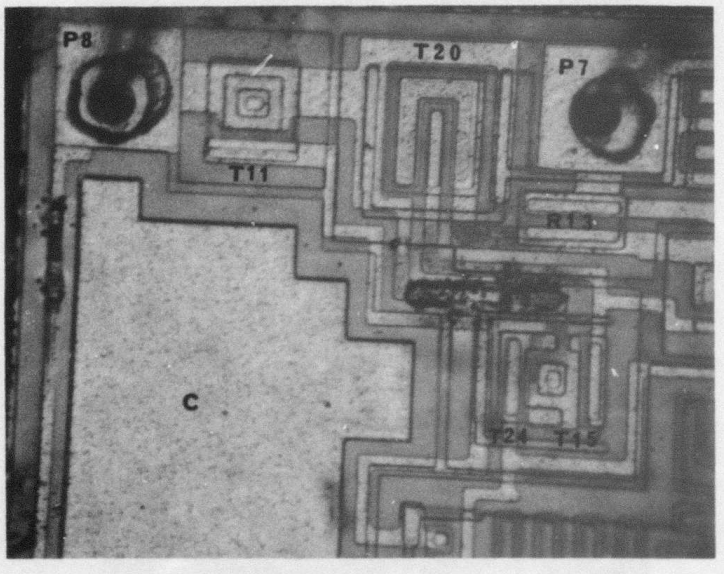

FIGURE 24 PHOTOMICROGRAPH OF METALLIZATION FAILURE WITH THE POSITIVE SUPPLY AS THE INJECTION PORT

Junction failures for pins 3, 4, 7, and 8 are shown in figures 25 through 28. There were no junction failures observed for pins 2 and 6, the offset null pins, or for pin 5, the negative supply pin. The junction failure usually shows melted metallization in the melt channel.

The most common junction failure was found in the input differential transistor pair T_1 - T_2. If the emitter-base junction of either transistor fails, the operational amplifier is only degraded. A collector-base junction failure in both transistors will cause a device failure because the two bases of the differential pair will be tied together through the common collector shared by both transistors. When both bases form a low-resistance path to the common collector, there is a resultant low-resistance path from base to base. Thus, the differential input is essentially shorted together and can not respond to an input.

Bond wire failures have been observed on pins 3, 4, 5, 6, 7, and 8. Figure 29 shows a bond wire failure at pin 4, and the others are similar. The bond wire failures like the metallization failures, are caused by Joule heating. When the DC current and the RF current dissipate enough heat in the bond wire, the wire melts and a metallic ball forms on the end of the wire where the molten metal settles after the break. With the 741, a bond wire failure on either offset null pin is insufficient to cause a catastrophic failure. The loss of either offset null bond wire will only degrade the device. Failures due to RF injected on these pins must also be related to some other cause. For example, with pin 6 as the RF entry port, the bond wires of both pins 6 and 7 were melted through at 5.6 GHz. Since pin 7 is the output, any loss of this bond wire is a failure.

Since the mechanisms of catastrophic failure and degradation are identical, the factors determining the severity of the damage are the location of the failure mechanism and the criticality of the component or circuit path damaged by the RF.

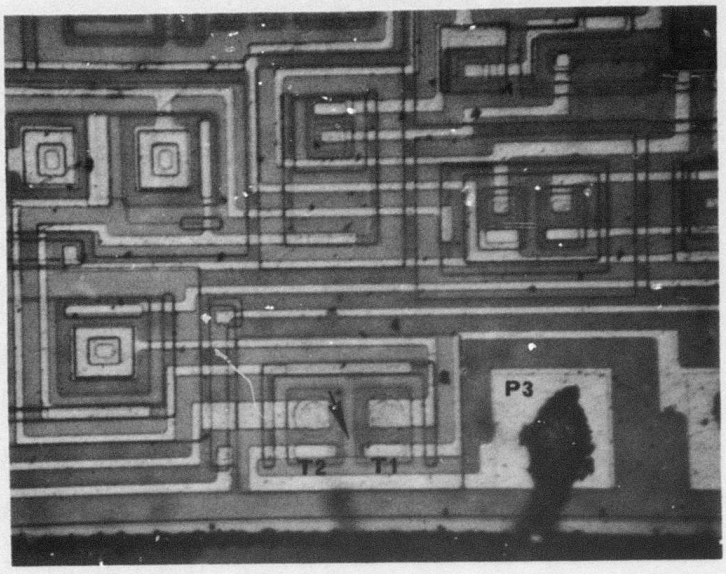

FIGURE 25 PHOTOMICROGRAPH OF JUNCTION FAILURE WITH THE INVERTING INPUT AS THE INJECTION PORT

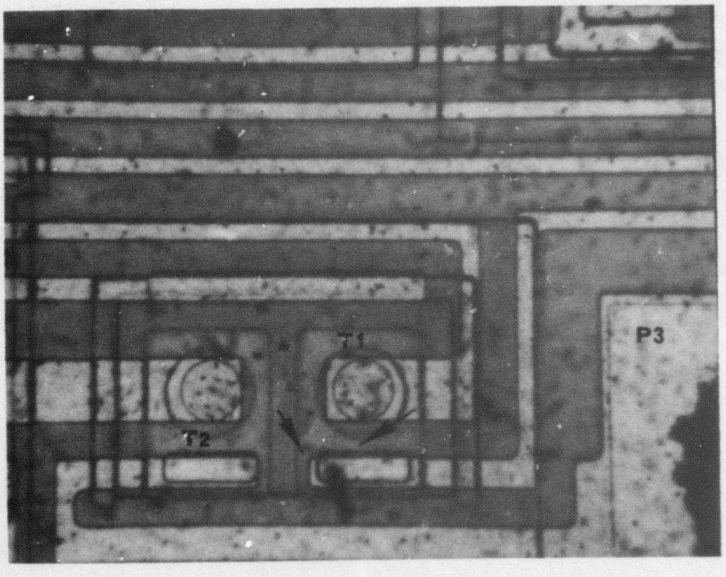

FIGURE 26 PHOTOMICROGRAPH OF JUNCTION FAILURE WITH THE NON-INVERTING INPUT AS THE INJECTION PORT

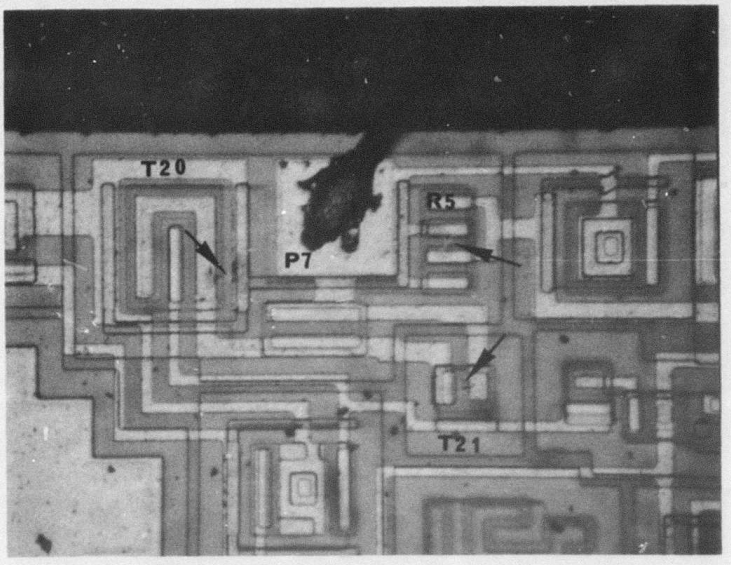

FIGURE 27 PHOTOMICROGRAPH OF JUNCTION FAILURE WITH THE OUTPUT AS THE INJECTION PORT

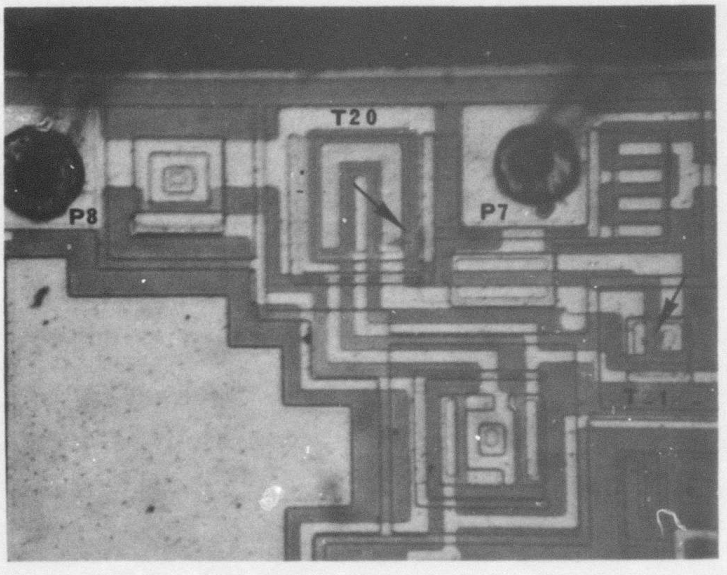

FIGURE 28 PHOTOMICROGRAPH OF JUNCTION FAILURE WITH THE POSITIVE SUPPLY AS THE INJECTION PORT

FIGURE 29 PHOTOMICROGRAPH OF BOND WIRE FAILURE WITH THE NON-INVERTING INPUT AS THE INJECTION PORT

2.3 Summary of RF Effects - The observed data showed that the 741 was very susceptible to RF power in the frequency range tested.

Figure 30 is a summary of worst-case 741 susceptibility data for interference and failure. These data were taken with the inverting input of the devices as the RF injection port since this was the most susceptible port. The threshold used for the interference curve was the RF power required to cause a ΔV of 0.5 volts in the output voltage. One-half volt ΔV was arbitrarily chosen as the interference threshold. The threshold level could have been chosen at any value of output voltage with a corresponding change in the plotted results. The failure threshold was the power required to cause the 741 to fail catastrophically.

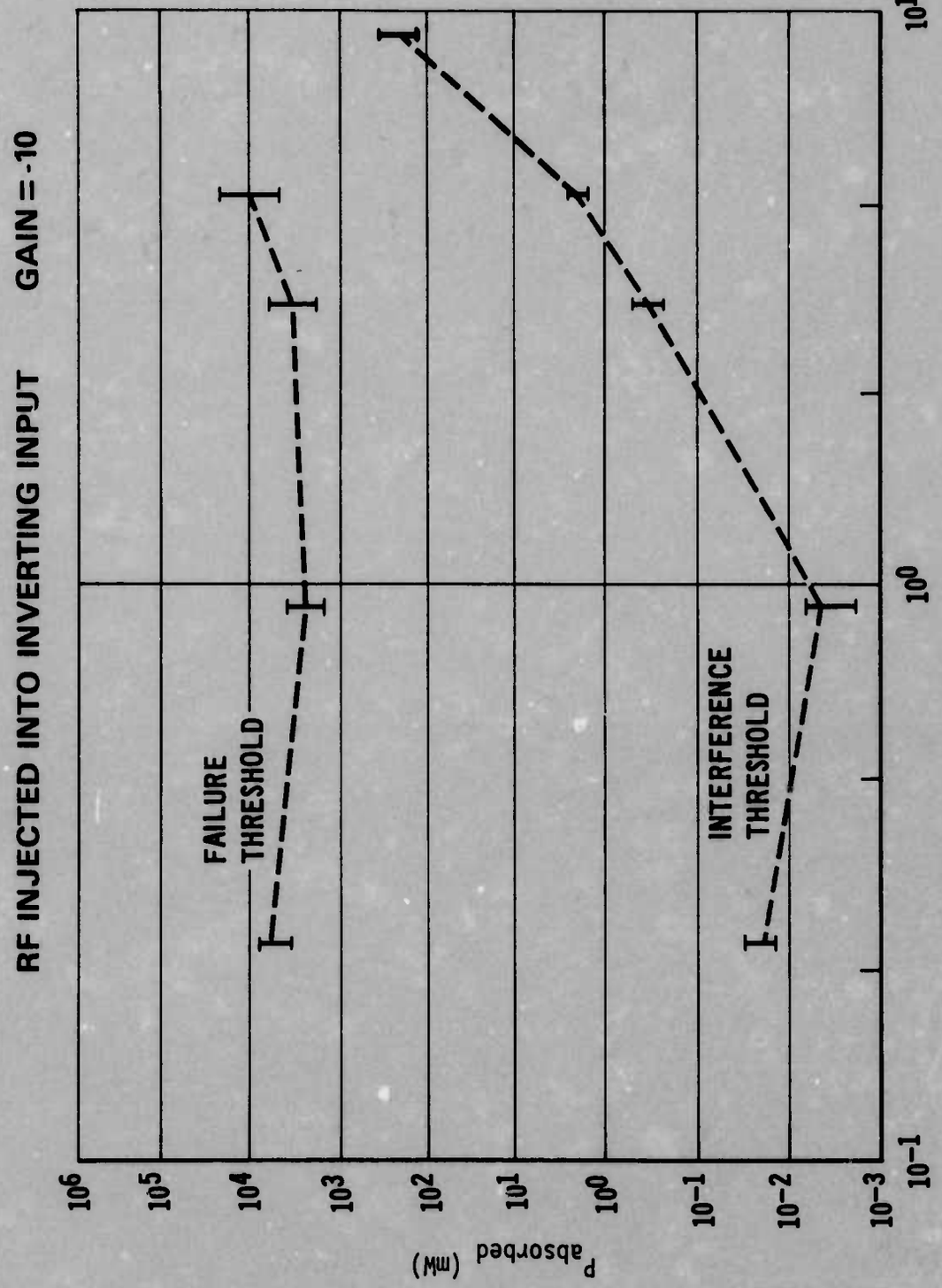

FIGURE 30 741 SUSCEPTIBILITY DATA SUMMARY

3. THEORY OF RF EFFECTS IN BIPOLAR DEVICES

As discussed in section 2, the injection of RF into the 741 causes the DC parameters to change during interference testing. The mechanism for these changes, as in all bipolar devices, is believed to be rectification in the various pn junctions of the device.

3.1 Rectification - Any pn junction is capable of rectification (but within certain limitations which are imposed by the physical characteristics of the junction). The limitations include frequency and power level, i.e,. the rectification efficiency depends on the frequency and drive level of the RF signal. In the 741, there are a multitude of pn junctions which can be divided into one of two categories, functional or parasitic. The functional junctions are those used to form transistors while the parasitic junctions are those which are inherent to the normal process of fabricating bipolar integrated circuits. For example, each p-channel resistor has a parasitic junction to substrate and each npn transistor collector has a parasitic junction to substrate. For a more detailed discussion of rectification in bipolar devices see "Bipolar NAND Gate Study", Report MDC E1123 (reference 2).

Figure 31 is a schematic diagram showing the parasitic diodes present in the 741. All of the device junctions can be expected to rectify coupled RF signals to some degree, but some sites will be more significant than others. In order to determine which junctions are the primary sites, a two-fold approach is used. First, the 741 interference data must be studied in detail to determine the exact change in the DC parameters under RF stimulus. Second, the DC response of each junction to RF is represented by a Norton equivalent generator as shown in figure 32. This representation of the pn junction under RF as a Norton generator is standard microwave practice [3]. From this approach, the primary rectification sites can be postulated so that a basic understanding of the observed interference data can be obtained.

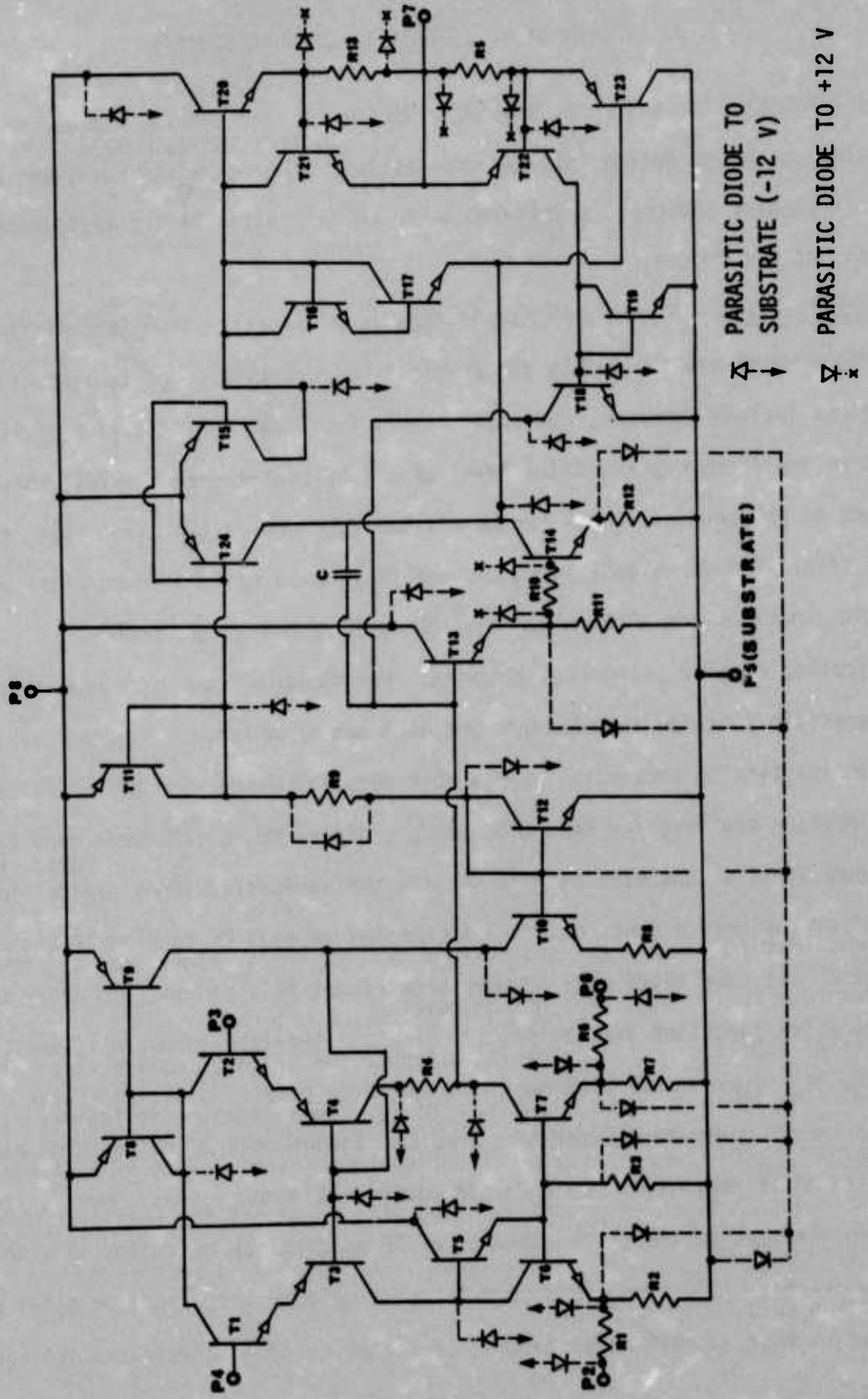

FIGURE 31 741 SCHEMATIC INCLUDING PARASITIC DIODES

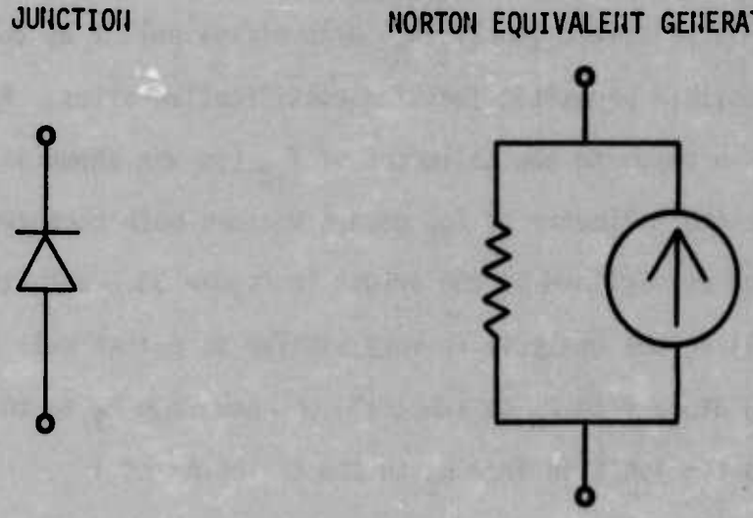

FIGURE 32 NORTON EQUIVALENT FOR PN JUNCTION

3.2 Interference Generators in 741 - As mentioned in section 2, the four ports most susceptible to RF are the two input ports and the two offset null ports. Since the other three ports are less susceptible by an order of magnitude or more, the generators for these ports will not be covered.

With RF applied to the noninverting input, the primary rectification site is believed to be the emitter-base junction of T_1. This location is logical because it is the first forward-biased junction which the RF sees. With RF applied to the inverting input, the primary recitification site is across the emitter-base junction of T_2. With the differential input circuit, this is the "mirror image" of the noninverting case.

With RF injected into either offset null port, there is no functional pn junction directly in the RF path. In these two cases, the RF is apparently rectified in parasitic junctions. With offset null 2 as the input port, there are several possible parasitic junction rectification sites. R_1 has a diode to substrate and R_2 has a diode to the collector of T_{12} (as was shown in figure 31). The junction from R_2 to the collector of T_{12} occurs because both components are diffused in the same island as outlined by the arrows in figure 33. With the RF injected into offset null 6, the analysis is very similar to offset null 2. As shown in figure 31, there is a diode from R_6 to substrate and one from R_7 to the collector of T_{12}, similar to the junction from R_2 to the collector of T_{12}.

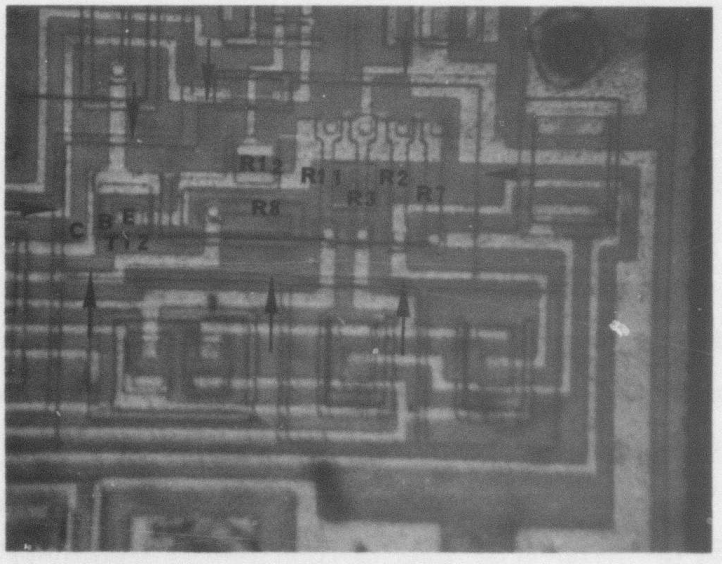

FIGURE 33 PHOTOMICROGRAPH OF 741 CHIP SHOWING THE T_{12} - RESISTOR ISLAND

4. ANALYSIS OF RF EFFECTS AND MODEL DEVELOPMENT

In this section, the interference susceptibility data from section 2 will be analyzed. The general rectification theory from reference 2 will be applied to the data. Together, the data and the general theory will be used to develop a plausible model for RF effects in the 741. However, only primary effects will be treated; higher-order effects such as the polarity switch from one saturation level to the other require further investigation.

4.1 Circuit Implications of Rectification in 741 - Each possible rectification site identified in section 3.2 will be studied by determining the effect of inserting its Norton generator on the 741 internal circuitry. The effect of the generator will then be compared to the actual interference data for the corresponding case. An explanation of the internal behavior of the 741 for DC and low frequency signals is given in Appendix B. This explanation of normal operation provides a background for the analysis of RF effects in the same circuitry.

4.1.1 RF Entering Input Ports - With RF applied to the noninverting input, the emitter-base junction of T_1 is believed to be the primary rectification site. Figure 34 shows the location of the Norton generator with the noninverting input as the RF injection port. The result of the addition of this generator to the circuit is an increase in the current in T_3. The increase in current due to the generator is exactly analagous to the normal operation explained in section B.2. Therefore, the result must be the same as discussed in Appendix B with the output voltage becoming more positive. Figure 35 shows that V_{out} does become more positive with increasing RF power into the noninverting input.

With RF applied to the inverting input, the emitter-base junction of T_2 is believed to be the primary rectification site. Figure 36 shows the Norton generator for this case. This is the "mirror image" of the noninverting case discussed above because of the differential input circuit.

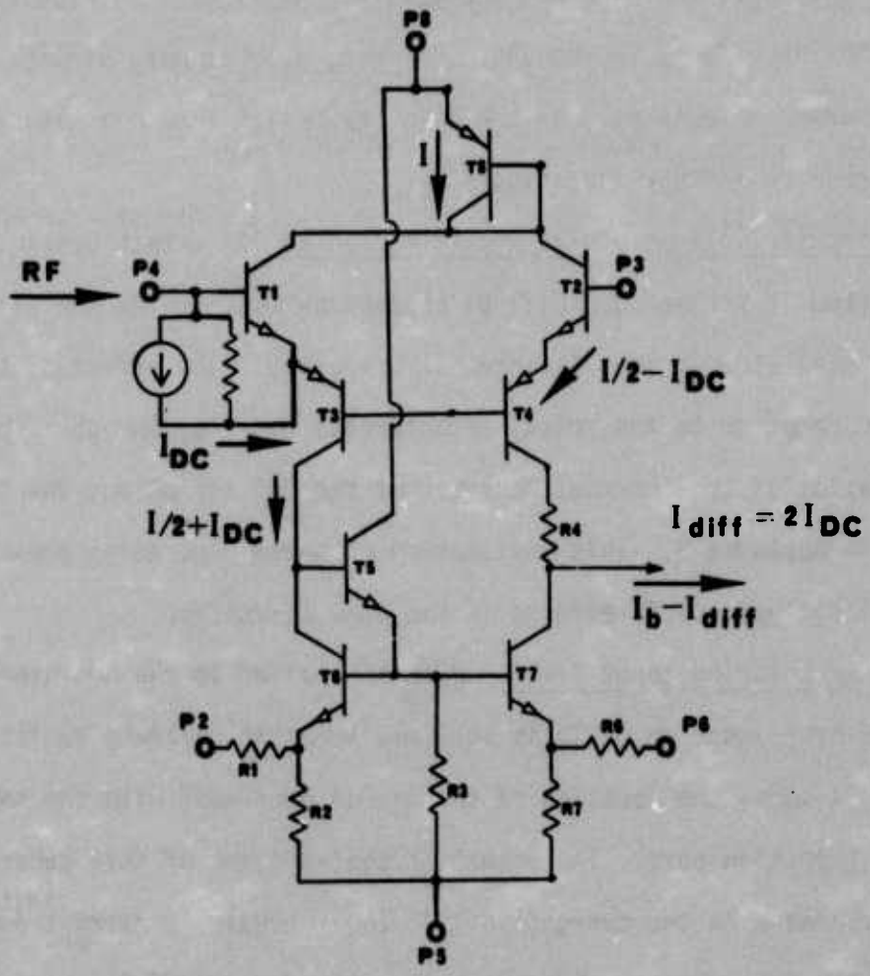

FIGURE 34 RF GENERATOR LOCATION WITH THE NON-INVERTING INPUT AS THE INJECTION PORT

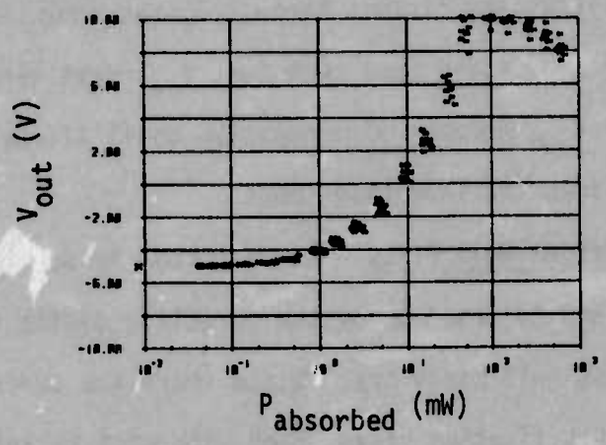

FIGURE 35 PLOT OF V_{out} VS $P_{absorbed}$ WITH THE NON-INVERTING INPUT AS THE INJECTION PORT AT 3.0 GHz

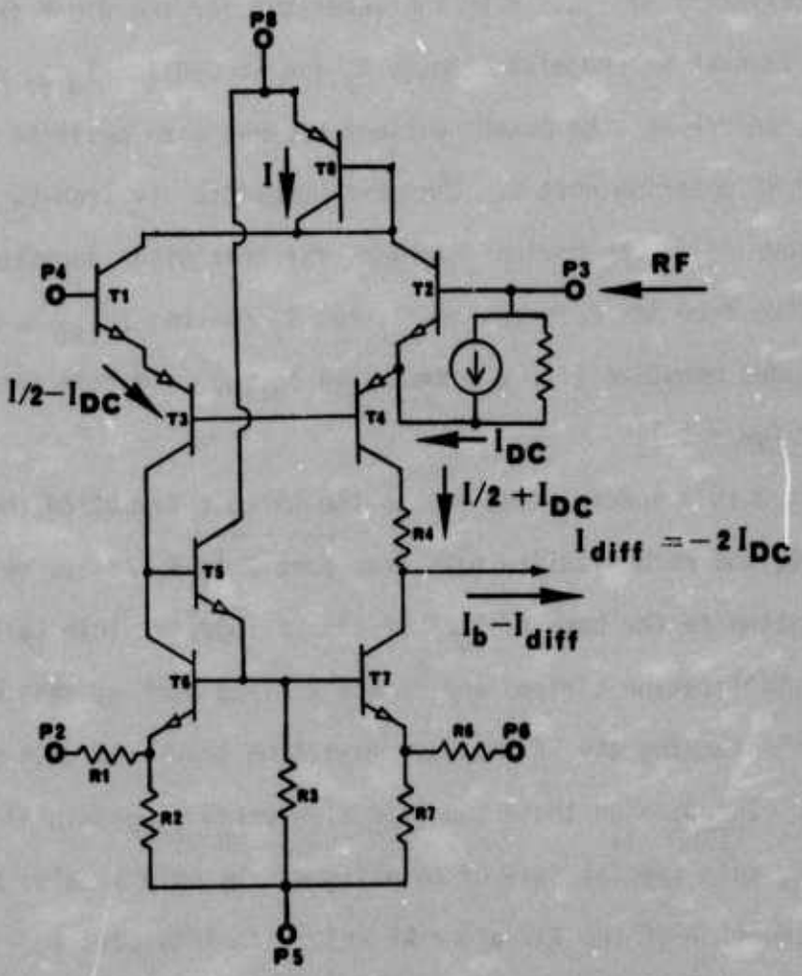

FIGURE 36 RF GENERATOR LOCATION WITH THE INVERTING INPUT AS THE INJECTION PORT

By similar analysis, the current through T_4 (as shown in figure 36) produces the reverse of the noninverting case such that V_{out} must become more negative. Figure 37 shows that V_{out} becomes more negative until it reaches saturation with increasing RF power into the inverting input.

4.1.2 RF Entering Offset Null Ports - As discussed in section 3.2, the primary rectification sites are believed to be the parasitic diodes from the resistor networks in the offset null circuitry. Since there are several possible parasitics which could be the rectification sites, each site will be analyzed.

Figure 38 shows two possible locations for the Norton generator with offset null port 2 as the injection port. R_1 has a diode to substrate and R_2 has a diode to the collector of T_{12}. A Norton generator for the diode from R_1 would increase current through R_2 and also through R_7 and T_7 causing I_{diff} to increase. However, if I_{diff} increases, the output voltage becomes more positive and this is not the case for RF entering port 2. The next parasitic is from R_2 to the collector of T_{12} (figure 38). The Norton generator for this diode decreases current from T_6 and R_2 and also from its matched-pair T_7 and R_7 causing I_{diff} to decrease. The output voltage goes negative (for a decrease in I_{diff}), and this is the case of RF entering port 2 (figure 39).

Port 2 is a special case due to the circuit layout on the chip. As shown in figure 40, the metallization path from port 2 to R_1 passes very close to the metallization to the base of T_2. If the RF injected into port 2 should couple across metallization stripes and inject RF into port 3, this would have the same effect as injecting the RF into the inverting input but with some loss due to coupling. The data on these two injection ports (Appendix A) uphold this supposition. Therefore, this special case of coupling on the chip is also a plausible explanation for the behavior of the 741 under RF injection into port 2.

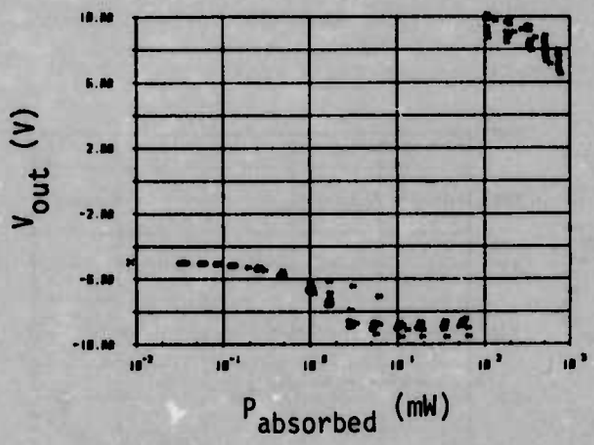

FIGURE 37 PLOT OF V_{out} VS $P_{absorbed}$ WITH THE INVERTING INPUT AS THE INJECTION PORT AT 3.0 GHz

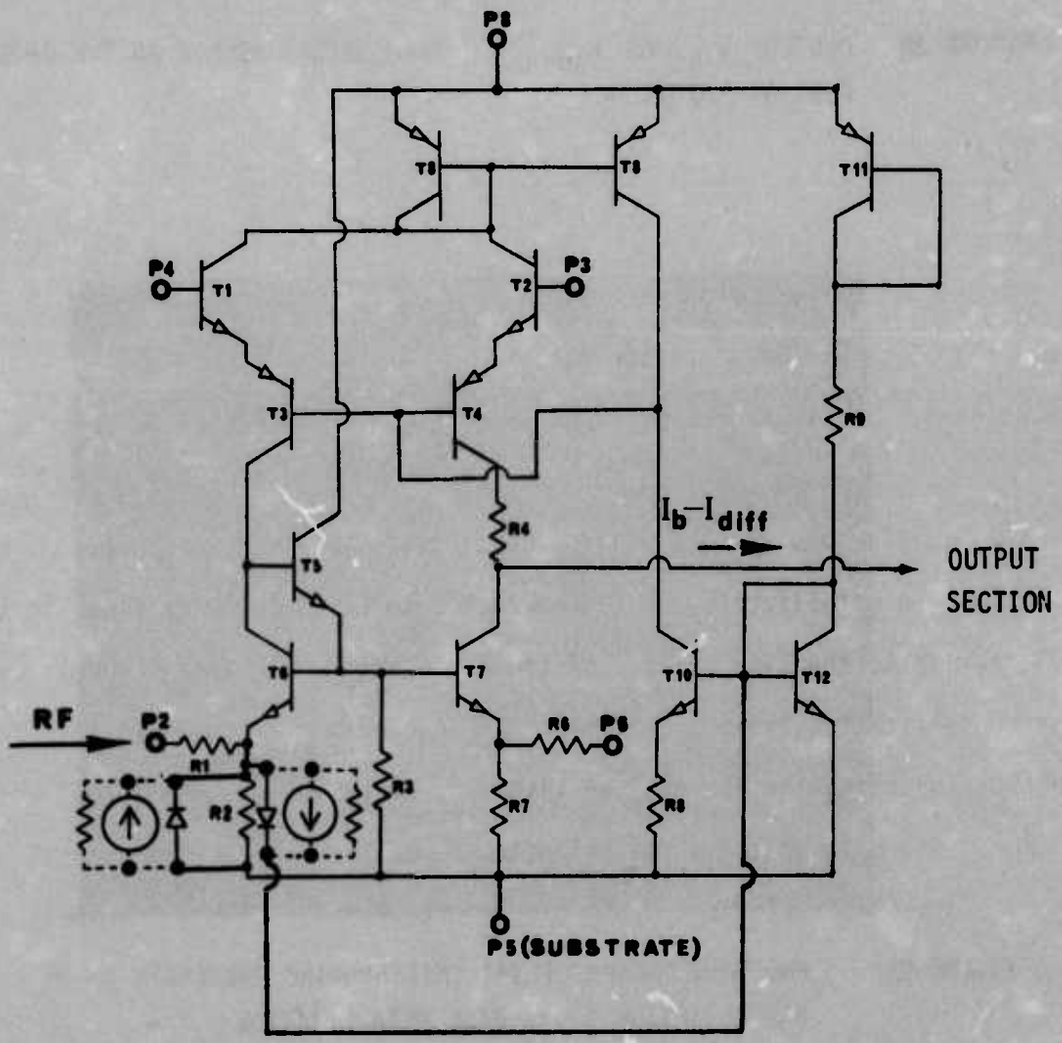

FIGURE 38 RF GENERATOR LOCATIONS WITH OFFSET NULL 2 AS THE INJECTION PORT

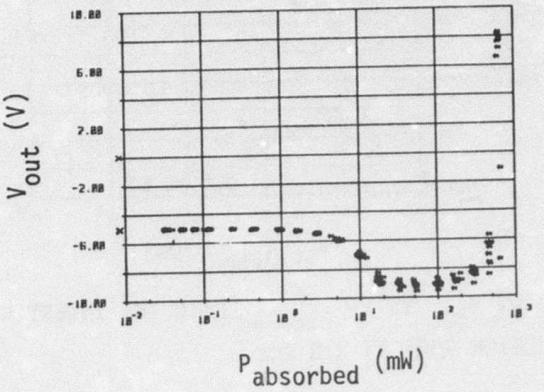

FIGURE 39 PLOT OF V_{out} VS $P_{absorbed}$ WITH OFFSET NULL 2 AS THE INJECTION PORT AT 3.0 GHz

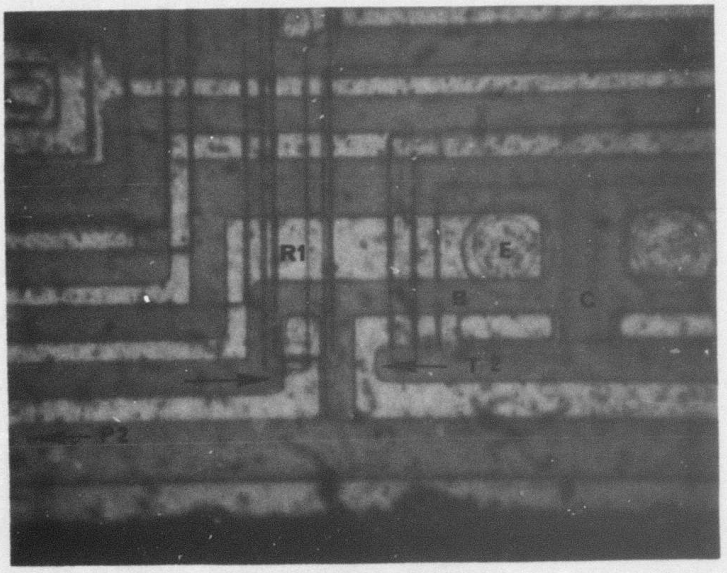

FIGURE 40 PHOTOMICROGRAPH OF 741 CHIP SHOWING PROXIMITY OF R_1 METALLIZATION TO T_2 BASE METALLIZATION

With offset null port 6 as the injection port, the two possible locations for a Norton generator are shown in figure 41. R_6 has a diode to substrate and R_7 has a diode to the collector of T_{12}, similar to the junction from R_2 to the collector of T_{12}. The Norton generator for the diode from R_6 to substrate causes the current in T_7 to decrease and I_{diff} to decrease. A decrease in I_{diff} causes the output voltage to go negative; however, the output voltage goes more positive with RF entering port 6 (figure 42). As with port 2, the next diode from R_7 to the collector of T_{12} is the parasitic which provides another rectification site. The Norton generator for this diode causes the current in T_7 to increase and I_{diff} to increase. The output voltage goes more positive with increasing I_{diff} so this generator causes the output voltage to move in the same direction as the experimental data (figure 42).

Although these rectification sites may not <u>definitely</u> cause the RF effects observed, they do provide a very plausible explanation of the effects.

4.2 <u>Input Offset Generator Model</u> - The foregoing heuristic arguments are useful for achieving a physical understanding of what happens in the 741 and will be helpful in planning further investigations, but they do not provide immediate help to the users of this very sensitive device. There is a much simpler model of the interference effects available which leads to a potentially useful relationship of device parameters and circuit parameters, but which has not yet been linked to the aforementioned physical processes.

Referring to a typical interference data listing (as in Table 1), it is readily observed that the voltage at the inverting input terminal varies significantly with the applied RF signal. In normal operation, this voltage is very near zero volts (a "virtual ground") due to the negative feedback used in typical circuit applications. Modelling the nonideal performance of the amplifier under interference conditions as an ideal differential amplifier with a series offset generator in the inverting input leg achieves a very satisfactory explanation of all the observed interference effects in the 741.

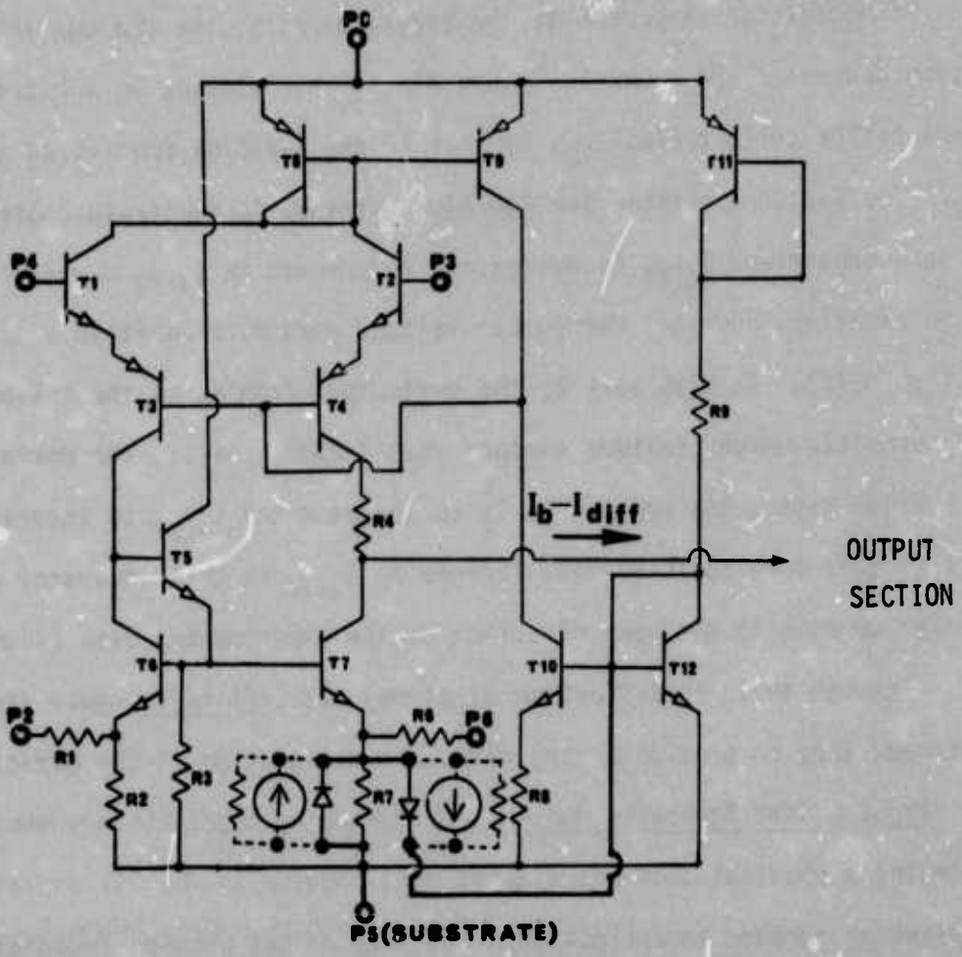

FIGURE 41 RF GENERATOR LOCATIONS WITH OFFSET NULL 6 AS THE INJECTION PORT

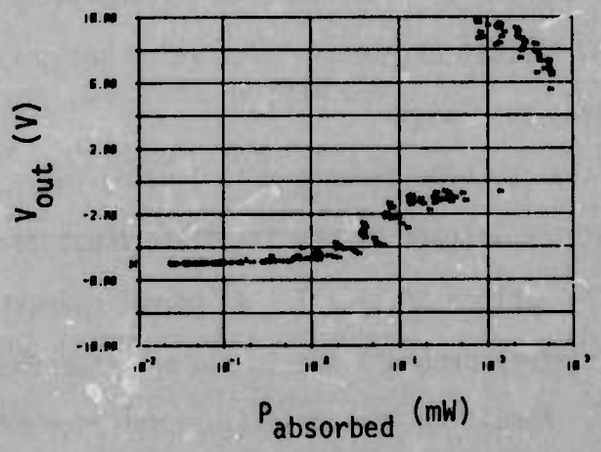

FIGURE 42 PLOT OF V_{out} VS $P_{absorbed}$ WITH OFFSET NULL 6 AS THE INJECTION PORT AT 3.0 GHz

Figure 43 shows the 741 amplifier circuit with the addition of the offset interference generator. The voltage V_{ii} provided by this generator to the inverting input is a function of the RF drive signal as revealed in the observed data. From figure 43, the voltage and current equations can be derived with the assumption that the amplifier is ideal:

$$I_{in} = - I_f \qquad \text{Assume } Z_{in} \sim \infty$$

$$V_{in} = I_{in} R_{in} + V_{ii} - V_e \qquad \text{Assume } V_e \sim 0$$

$$I_f = \frac{V_{out} - V_{ii}}{R_f}$$

The combination of these three equations into one gives:

$$V_{in} = \frac{-V_{out} + V_{ii}}{R_f} R_{in} + V_{ii}$$

or:

$$V_{out} = - \frac{R_f}{R_{in}} V_{in} + \frac{R_f + R_{in}}{R_{in}} V_{ii} \qquad (1)$$

Figure 44 is a combined plot of theoretical and observed values of equation 1. The solid line is the theoretical value for equation 1 with constant V_{in} equal to 0.5 volt and the saturation limits imposed by the interference test configuration used. The plotted points are from a typical data run consisting of 10 devices. This particular case was observed with RF applied to the noninverting input at 0.91 GHz and the correlation is seen to be excellent. In fact, for every case tested, the observed data show this same excellent correlation, regardless of injection port or frequency.

Equation 1 permits the system designer to assess the impact of his choice of feedback levels on the circuit susceptibility if the character of the RF interference signal is known. For instance, a CW interference signal will result in a constant offset at the output which can be minimized by cutting the circuit

gain. Of course, the impact of cutting the gain must be assessed on the normal signal as well. Equation 1 will account for pulsed interference if the time-dependent nature of the interfering signal is merely translated to a time-modulated interference signal.

In order to use equation 1 to predict the interference effects, the designer must have an estimate of V_{ii} in terms of the RF signal present. The only method of obtaining V_{ii} at this time is to measure it empirically. The plots in figure 45 show measured values of V_{ii} as a function of absorbed RF power at the five test frequencies. The plots of V_{ii} vs $P_{absorbed}$ for the inverting input were chosen because the inverting input is the most susceptible port and these values of V_{ii} will be worst-case values. Therefore the designer has sufficient information to use equation 1 to estimate the impact of his choice of feedback levels on circuit susceptibility for a 741.

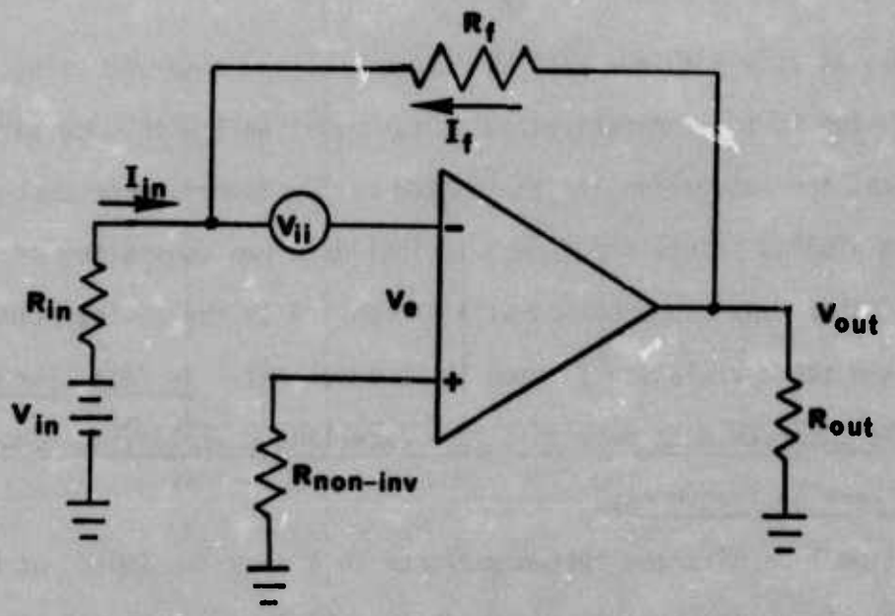

FIGURE 43 741 AMPLIFIER CIRCUIT INCLUDING OFFSET GENERATOR

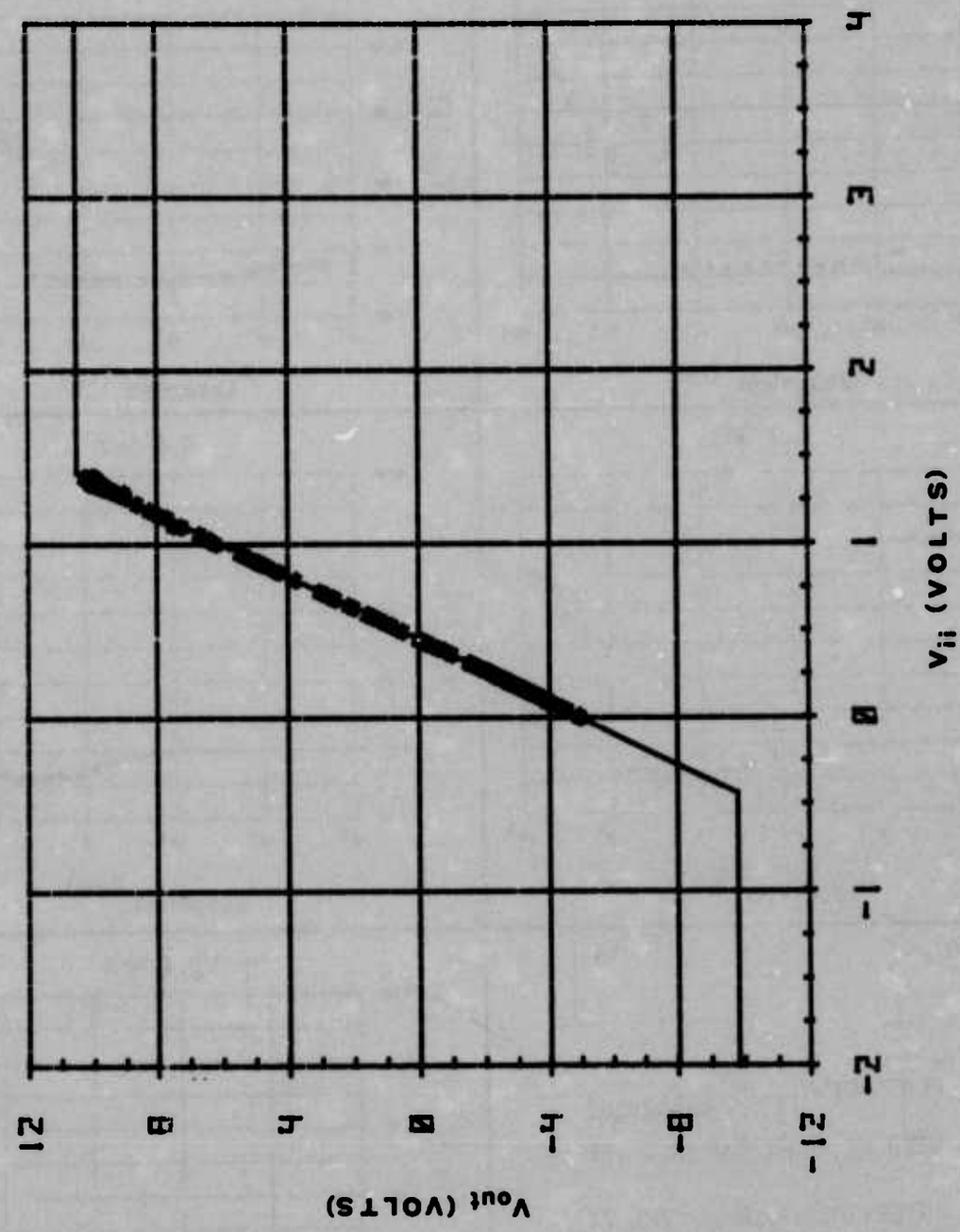

FIGURE 44 PLOT OF V_{out} VS. V_{ii} FOR PREDICTED AND OBSERVED VALUES WITH THE NON INVERTING INPUT AS THE INJECTION PORT AT 0.91 GHz

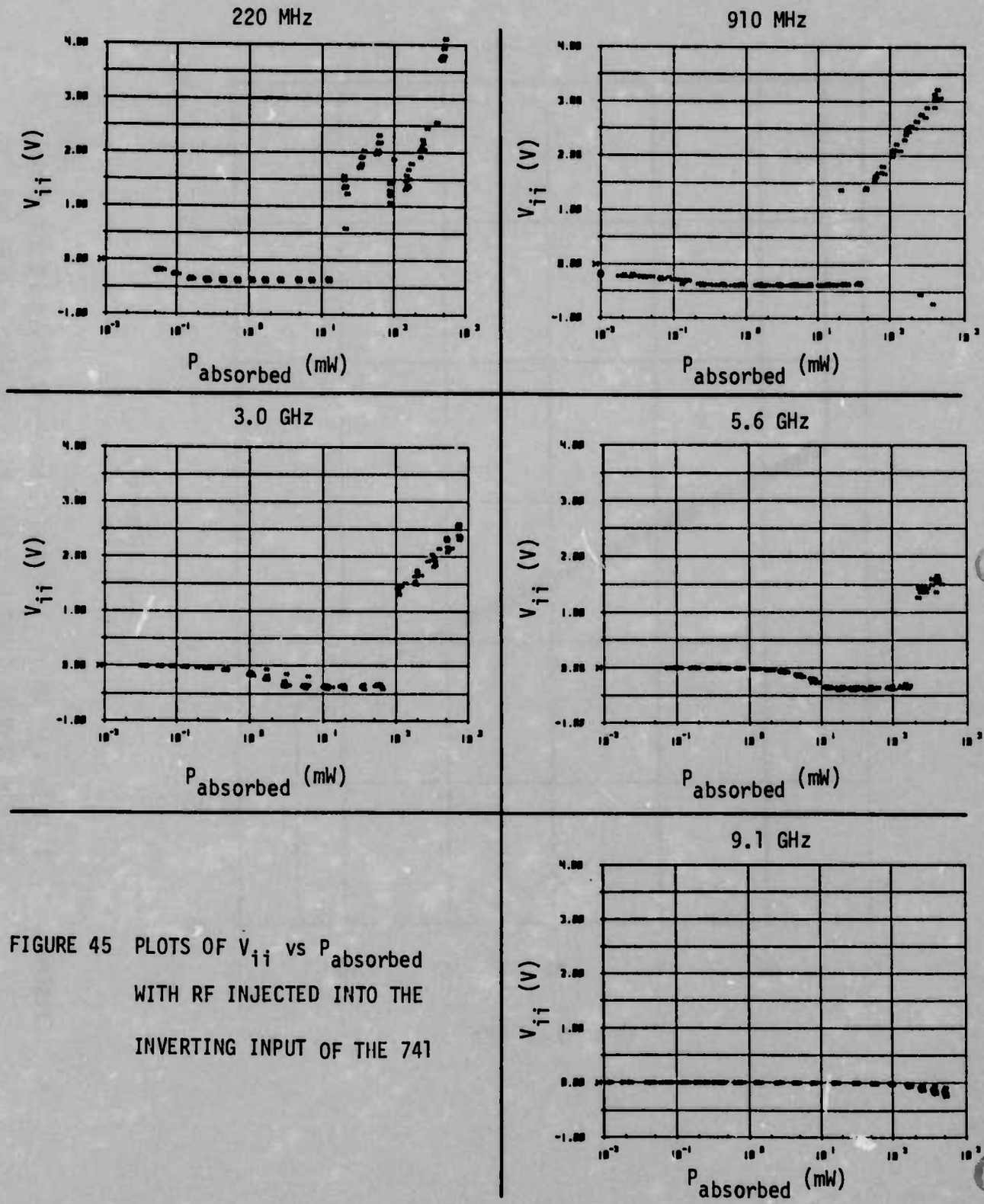

FIGURE 45 PLOTS OF V_{ii} vs $P_{absorbed}$ WITH RF INJECTED INTO THE INVERTING INPUT OF THE 741

5. CONCLUSIONS

From the observed data, the 741 demonstrates that it is highly susceptible to RF interference. Since it is so susceptible, all efforts should be made to isolate it from high-level RF fields. If a string of amplifiers is used to amplify a low-level signal, the first amplifier might serve as a buffer amplifier with a gain of one to cut down on the RF effects, especially in a dc-coupled circuit.

The analysis of the primary RF effects presented is based on the best information available. This information is limited because there are so few entry ports for monitoring the effects throughout such a large circuit. The major problem in analyzing the RF effects is taking into account the RF coupling on the chip. Therefore, while a precise analysis of the RF effects could not be accomplished, the analysis provided is plausible, explains the observed data, and follows normal circuit theory whenever possible.

There are still many areas of linear integrated circuit susceptibility which need additional study, specifically some of the secondary RF effects. However, in this single case of one device, one manufacturer, one date code, and one package style, the interference, degradation, and failure levels have been characterized and the preliminary analysis of the test data has been completed.

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3. E. L. Ginzton, Microwave Measurements, New York, McGraw-Hill Book Company, Inc., 1957

APPENDIX A

741 V_{out} vs $P_{absorbed}$ PLOTS

741 INTERFERENCE DATA

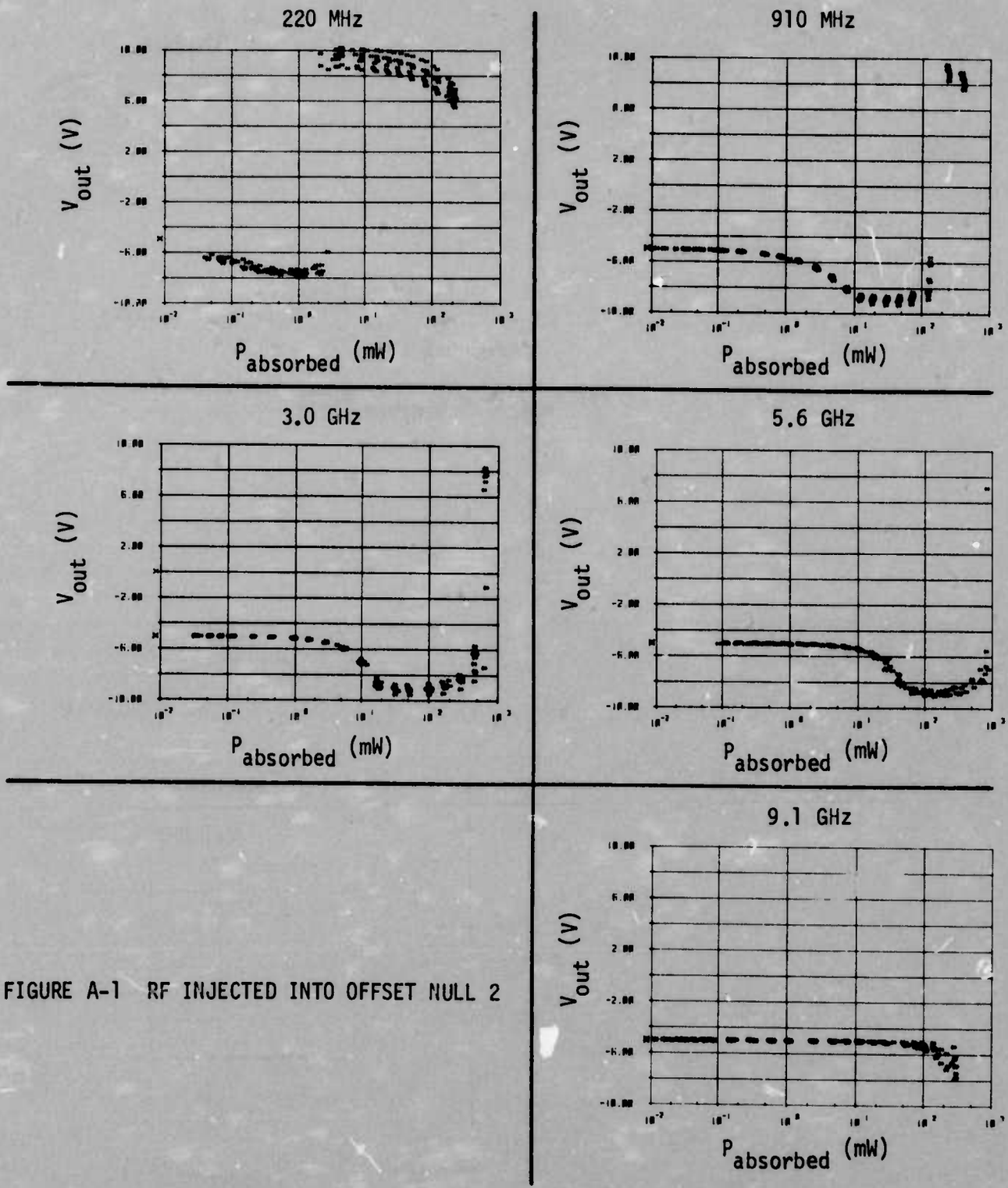

FIGURE A-1 RF INJECTED INTO OFFSET NULL 2

741 INTERFERENCE DATA

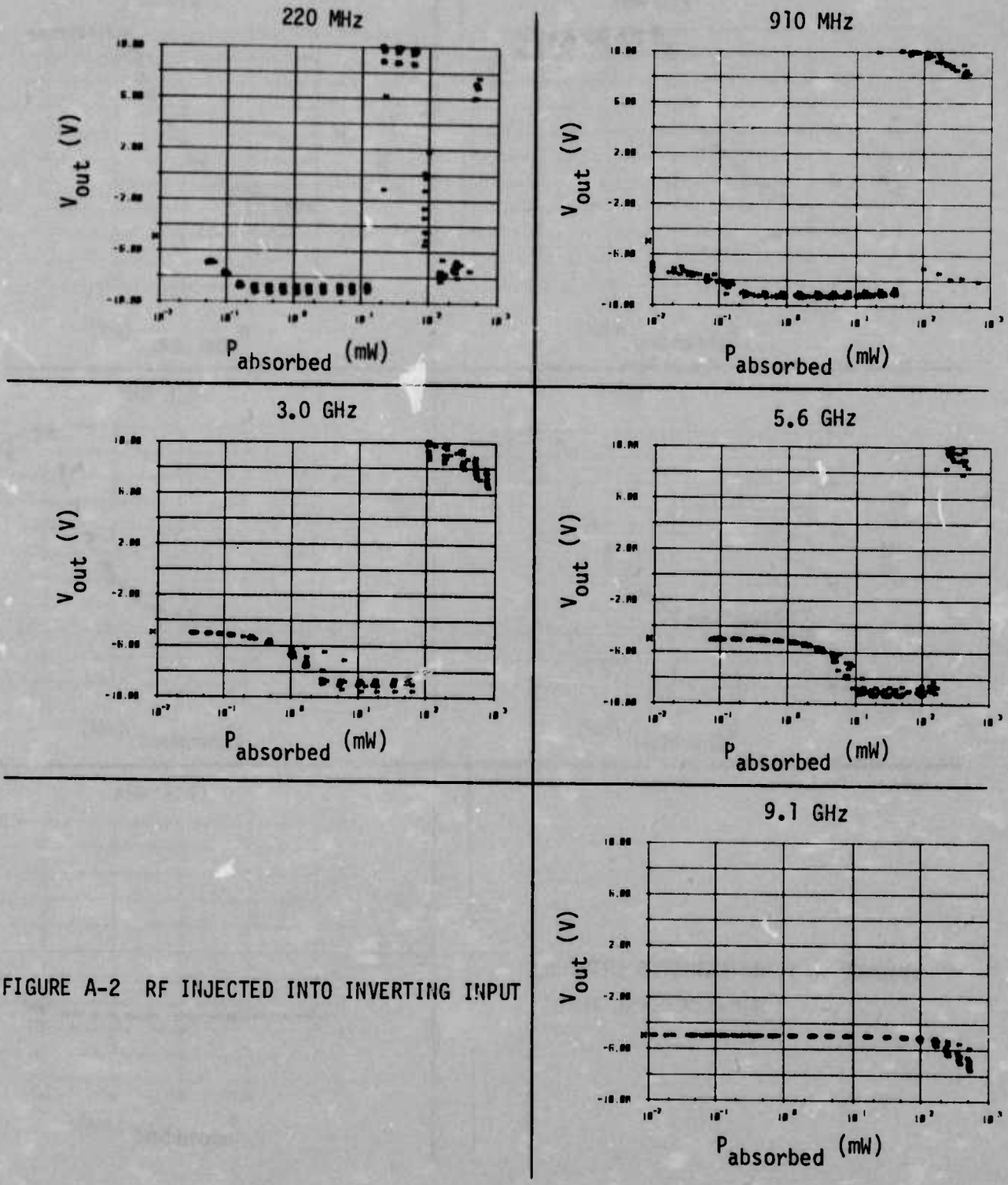

FIGURE A-2 RF INJECTED INTO INVERTING INPUT

741 INTERFERENCE DATA

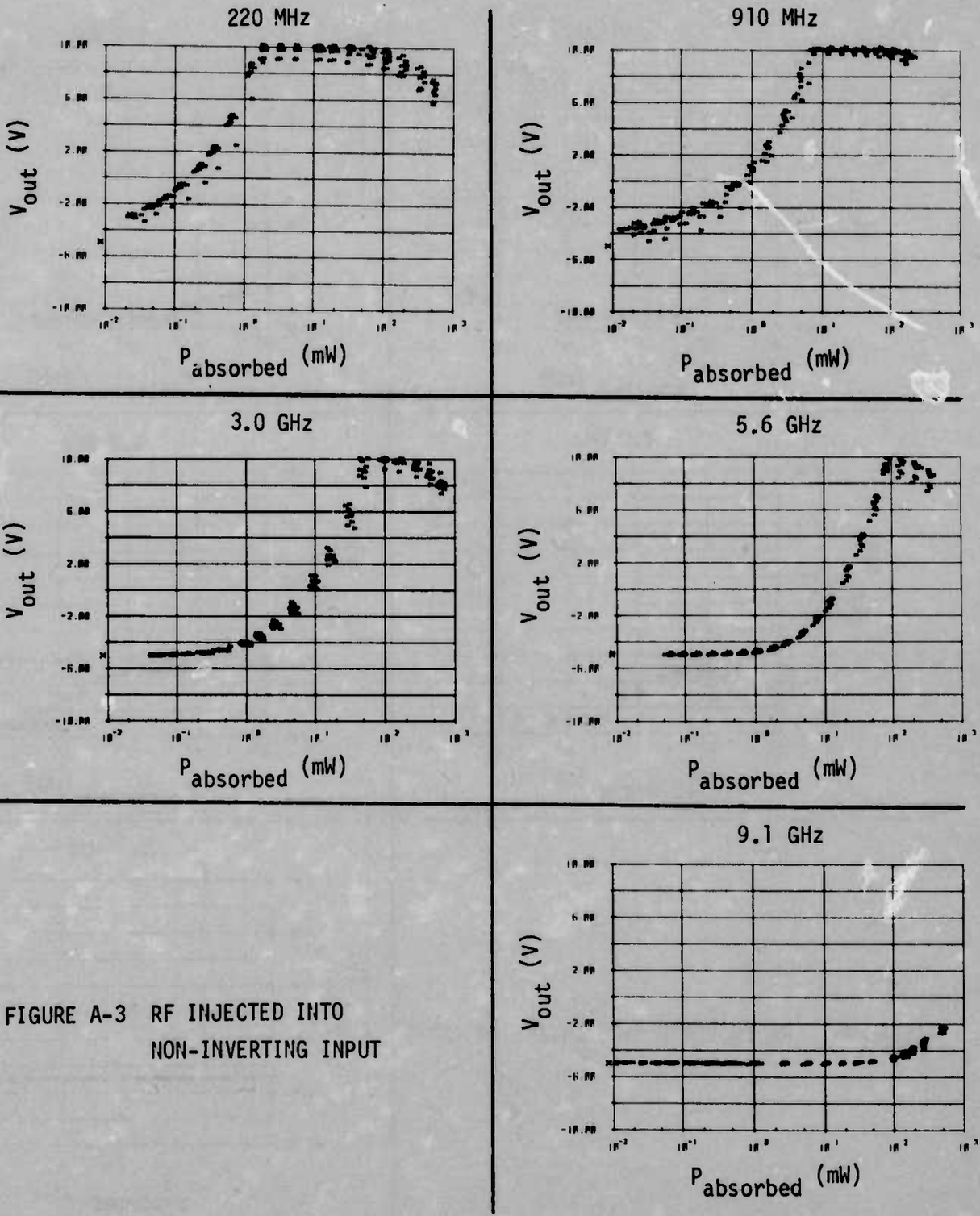

FIGURE A-3 RF INJECTED INTO NON-INVERTING INPUT

741 INTERFERENCE DATA

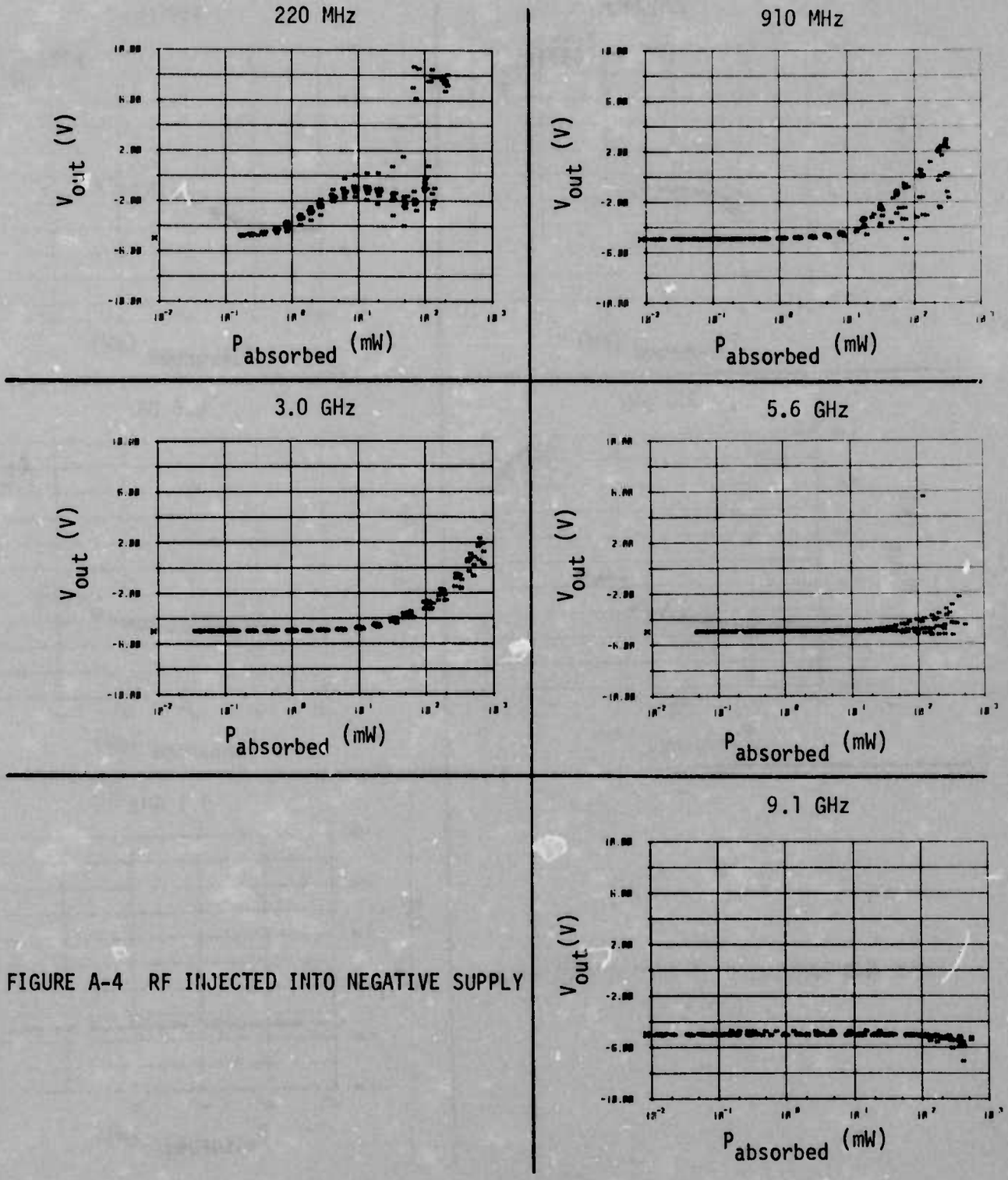

FIGURE A-4 RF INJECTED INTO NEGATIVE SUPPLY

741 INTERFERENCE DATA

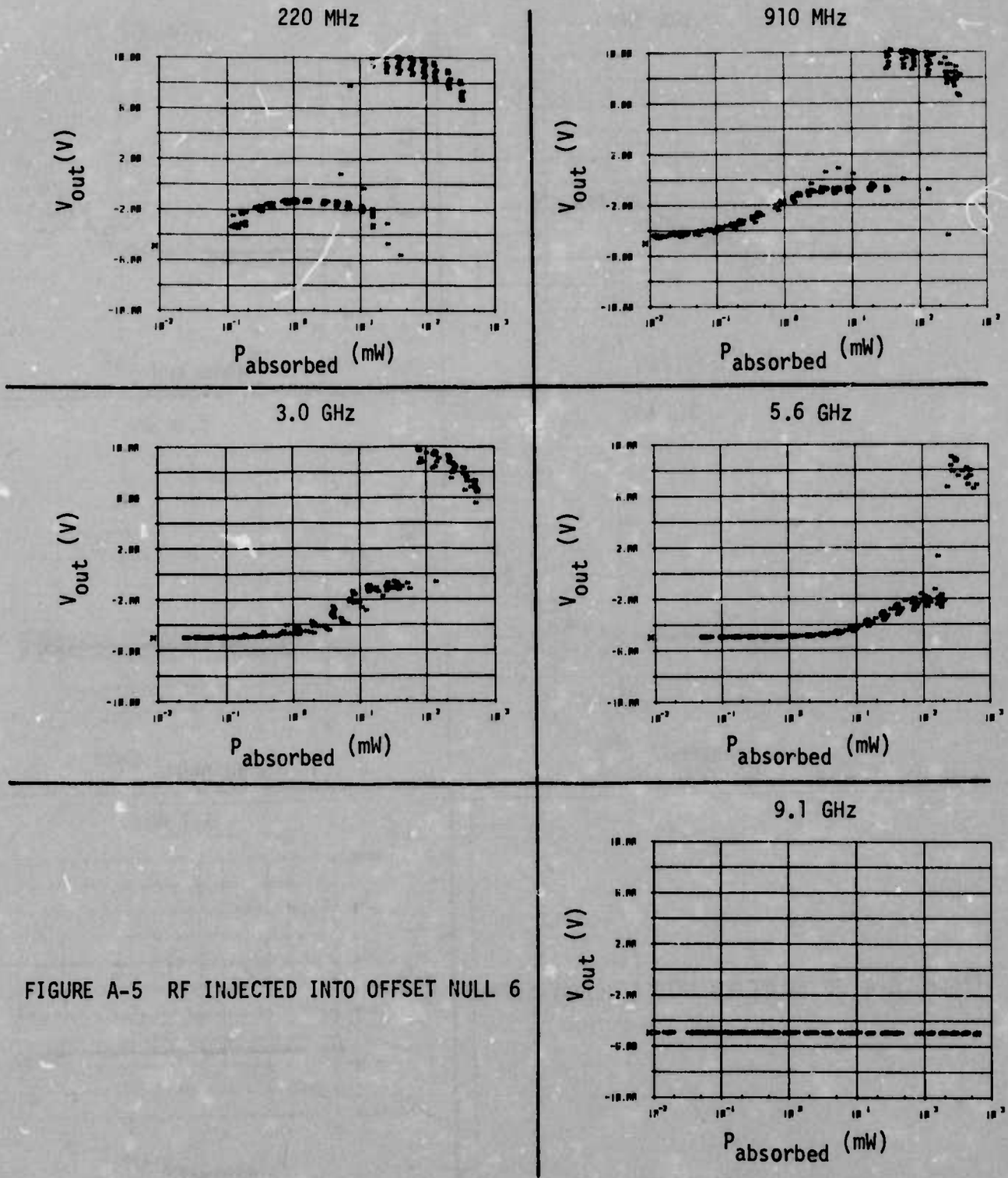

FIGURE A-5 RF INJECTED INTO OFFSET NULL 6

741 INTERFERENCE DATA

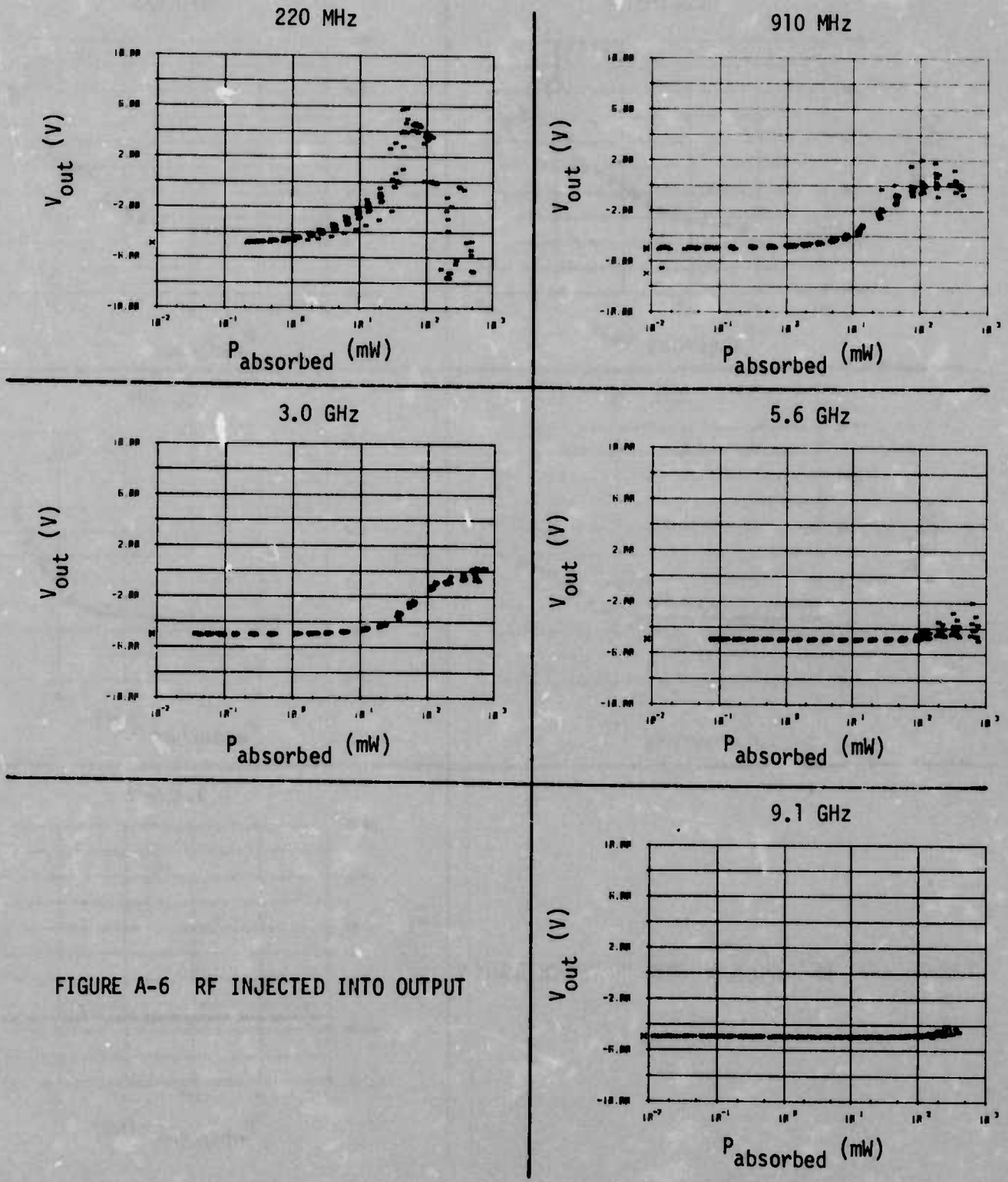

FIGURE A-6 RF INJECTED INTO OUTPUT

741 INTERFERENCE DATA

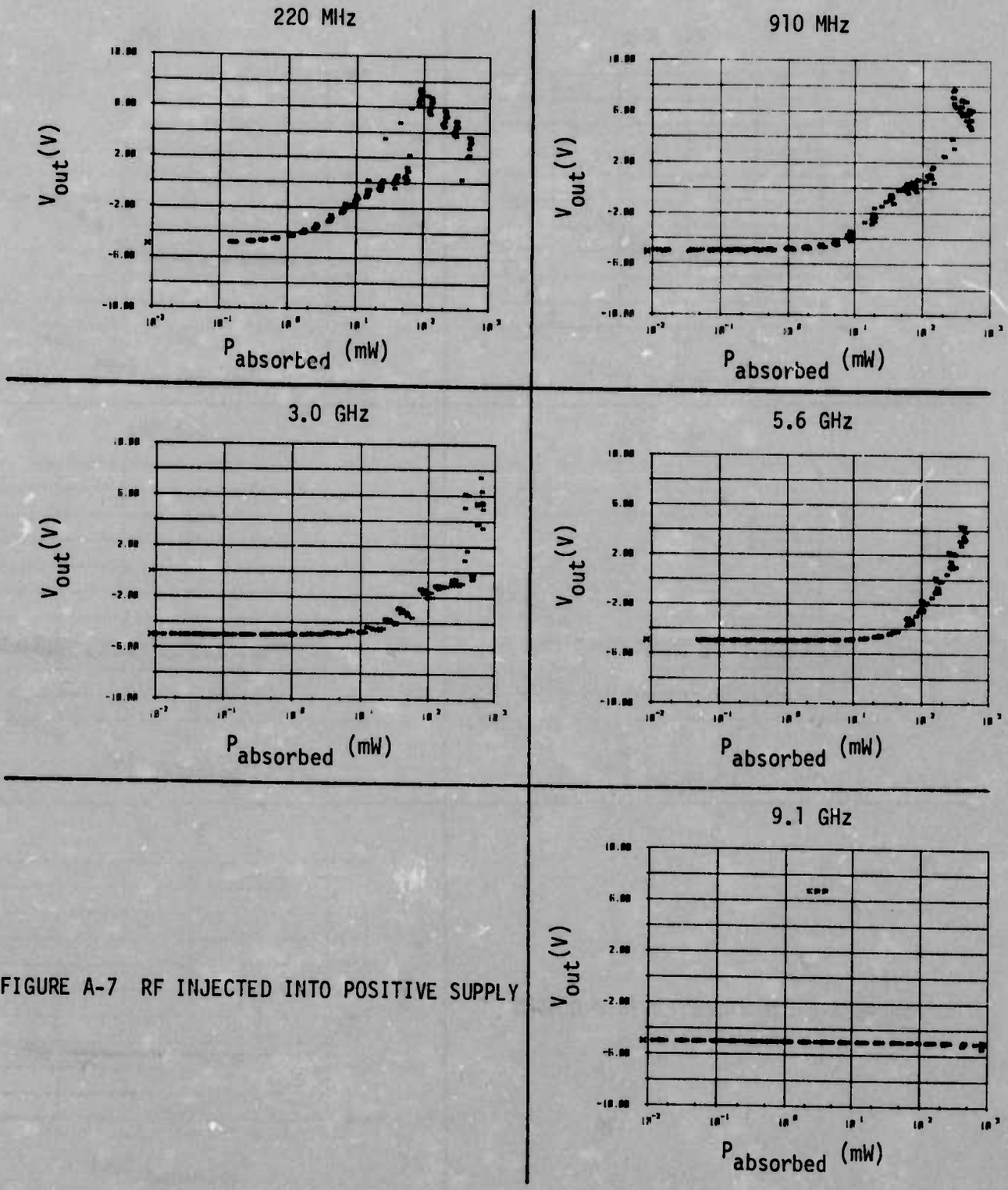

FIGURE A-7 RF INJECTED INTO POSITIVE SUPPLY

APPENDIX B

THEORY OF OPERATION OF 741

B. THEORY OF OPERATION

The 741 operational amplifier is a complex electronic circuit made up of 23 transistors, 13 resistors, and 1 capacitor. In order to explain the RF effects internal to the device, it is necessary first to know the normal dc and low frequency behavior internal to the device.

B.1 741 Block Diagram - Figure B-1 is a block diagram of the 741 internal circuitry (shown in figure 8). There are four basic blocks of the diagram: the differential amplifier, the balance, the high-gain amplifier, and the complementary output blocks. The other blocks support the basic blocks. These support blocks include two current-limiters, four current sources, and five voltage reference blocks. The arrows on the diagram indicate the signal flow from the input, through the device, to the output. The block diagram is divided into two basic parts, input and output, with only the voltage reference T_{11} - R_9 shared by both.

B.2 741 Circuit Operation - The 741 is a monolithic integrated circuit which utilizes matched-pair transistors, jumper resistors, a minimum number of resistors, and the smallest value of capacitance possible. The 741 has a high open-circuit gain (50,000 minimum) which is controlled with feedback in the external circuitry.

The input half of the block diagram is shown schematically in figure B-2. This input section converts the difference of two input voltages, V_{ii} and V_{ni}, to a current, I_b - I_{diff} which is the output for this section.

The voltage references and current sources in the input section provide a constant current I to the differential input pair T_1 and T_2. With the inputs shorted, an external offset null potentiometer is adjusted such that the output voltage of the 741 is zero. In order for the output voltage to be zero, the current out of node A must be I_b (the base current for T_{13} which just balances the output circuitry). I_b is the difference between the currents in T_1 and T_2 in the nulled

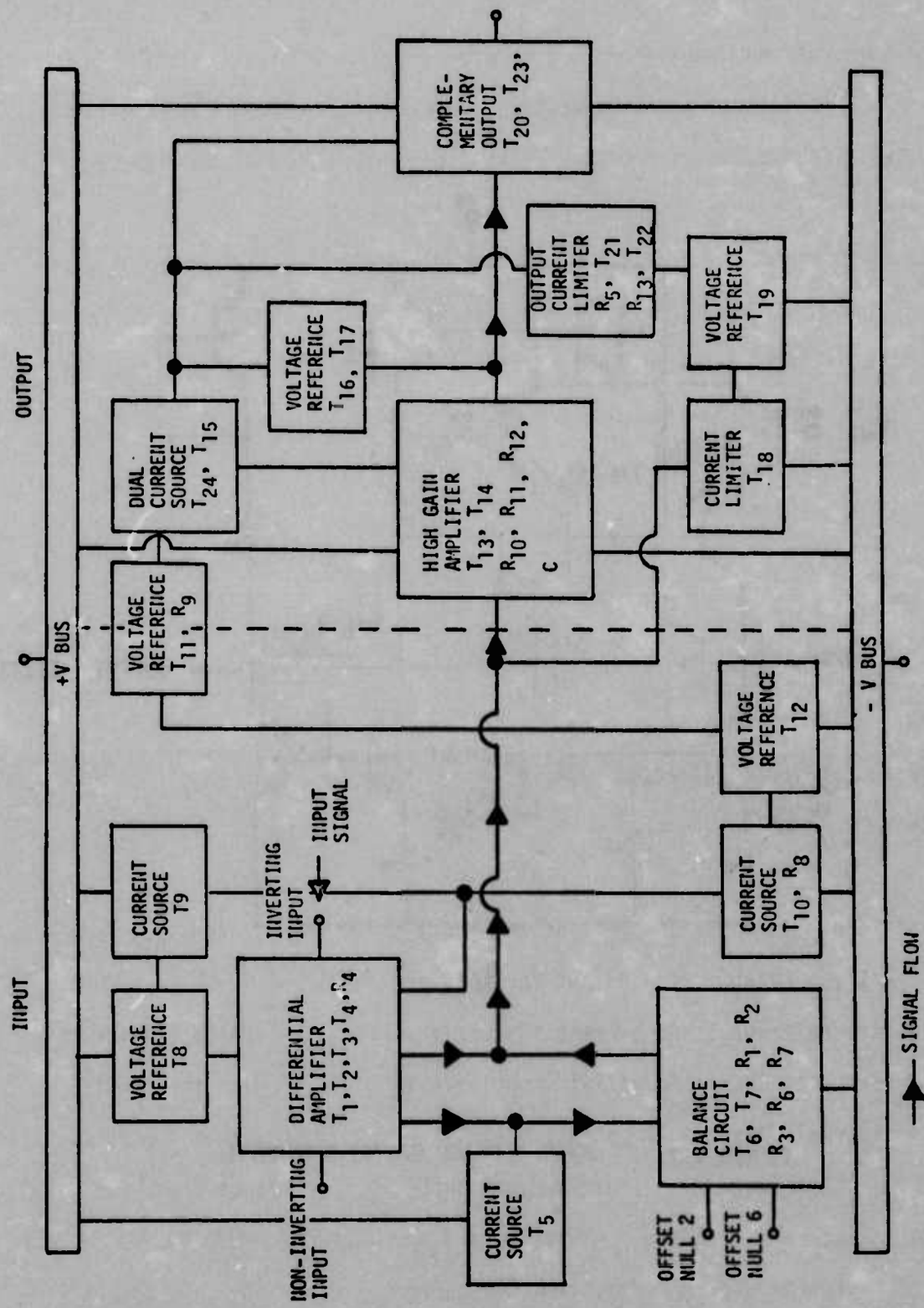

FIGURE B-1 BLOCK DIAGRAM OF 741 CIRCUIT

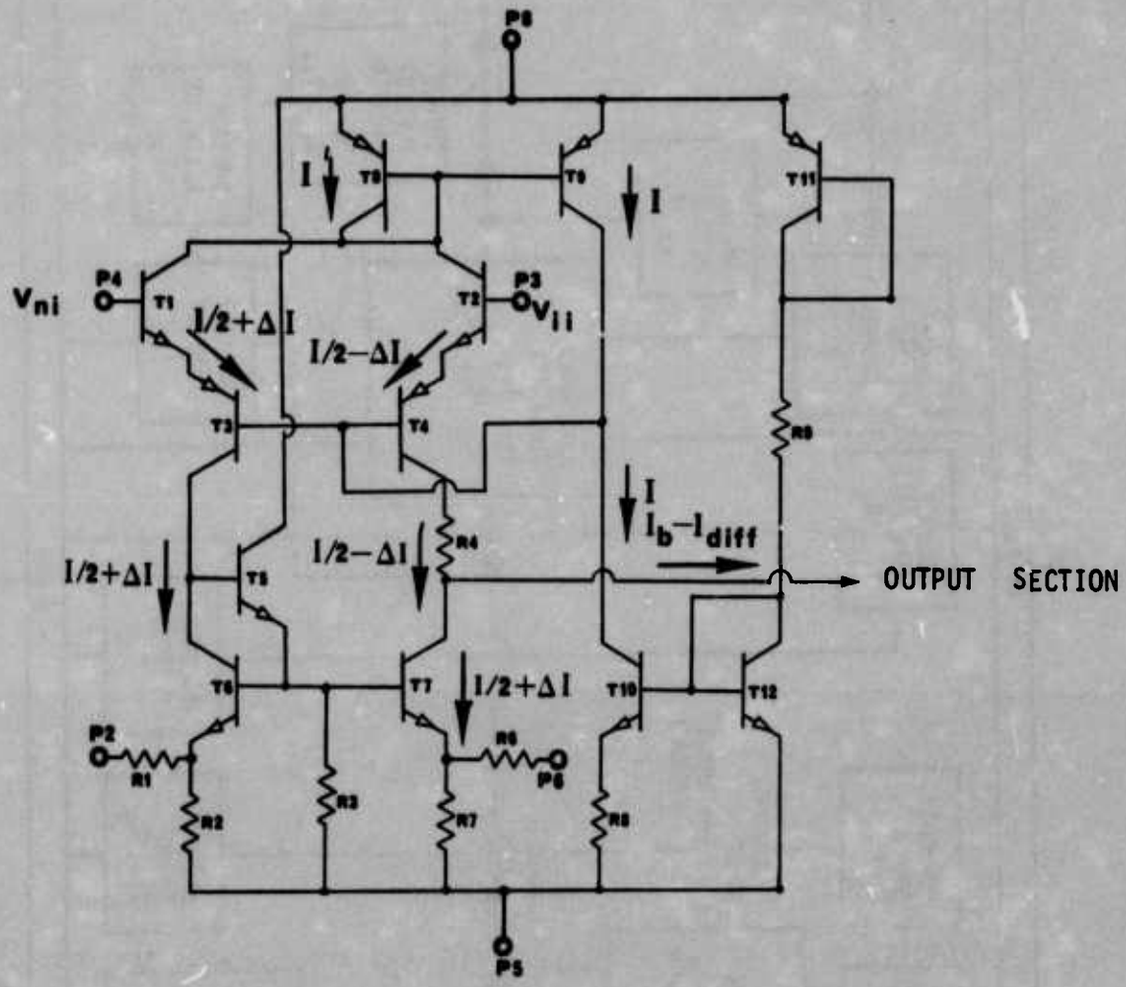

FIGURE B-2 INPUT SECTION OF 741 SCHEMATIC

condition. Since I_b is the null condition, it will be ignored for this analysis and the currents in T_1 and T_2 will be assumed equal to I/2.

If V_{ni} is not equal to V_{ii}, the currents in T_1 and T_2 are no longer equal to I/2. If V_{ni} is greater than V_{ii}, there will be an I/2 increase (ΔI) through T_1 and T_3 and a corresponding I/2 decrease ($-\Delta I$) through T_2 and T_4 since the total current I is constant. The current (I/2) + ΔI flows through T_6 and R_2. Since T_6 and T_7 are a matched-transistor pair and R_2 and R_7 are a matched-resistor pair, the current through T_7 and R_7 is also (I/2) + ΔI from node A because the bases are tied together. (I/2) - ΔI flows through T_2, T_4, and R_4 to node A. R_4 is used as a low resistance jumper path for ease of fabrication and has no effect on the normal operation of the circuit. At node A the equation is:

$$(I/2 - \Delta I)_{T_4} - (I/2 + \Delta I)_{T_7} + I_{diff} = 0$$

which reduces to:

$$I_{diff} = 2\Delta I.$$

With I_b as the null condition current and I_{diff} as the signal current, the total current to the output section is $I_b - 2\Delta I$.

The output section of the block diagram is shown schematically in figure B-3. This section converts the signal, which is I_{diff} to V_{out} after amplifying it by a factor of 50,000. The current amplification takes place in T_{13} and T_{14} and the conversion to voltage occurs in T_{16}, T_{17}, T_{20}, and T_{23} with the rest of the circuitry providing current limiting for the output.

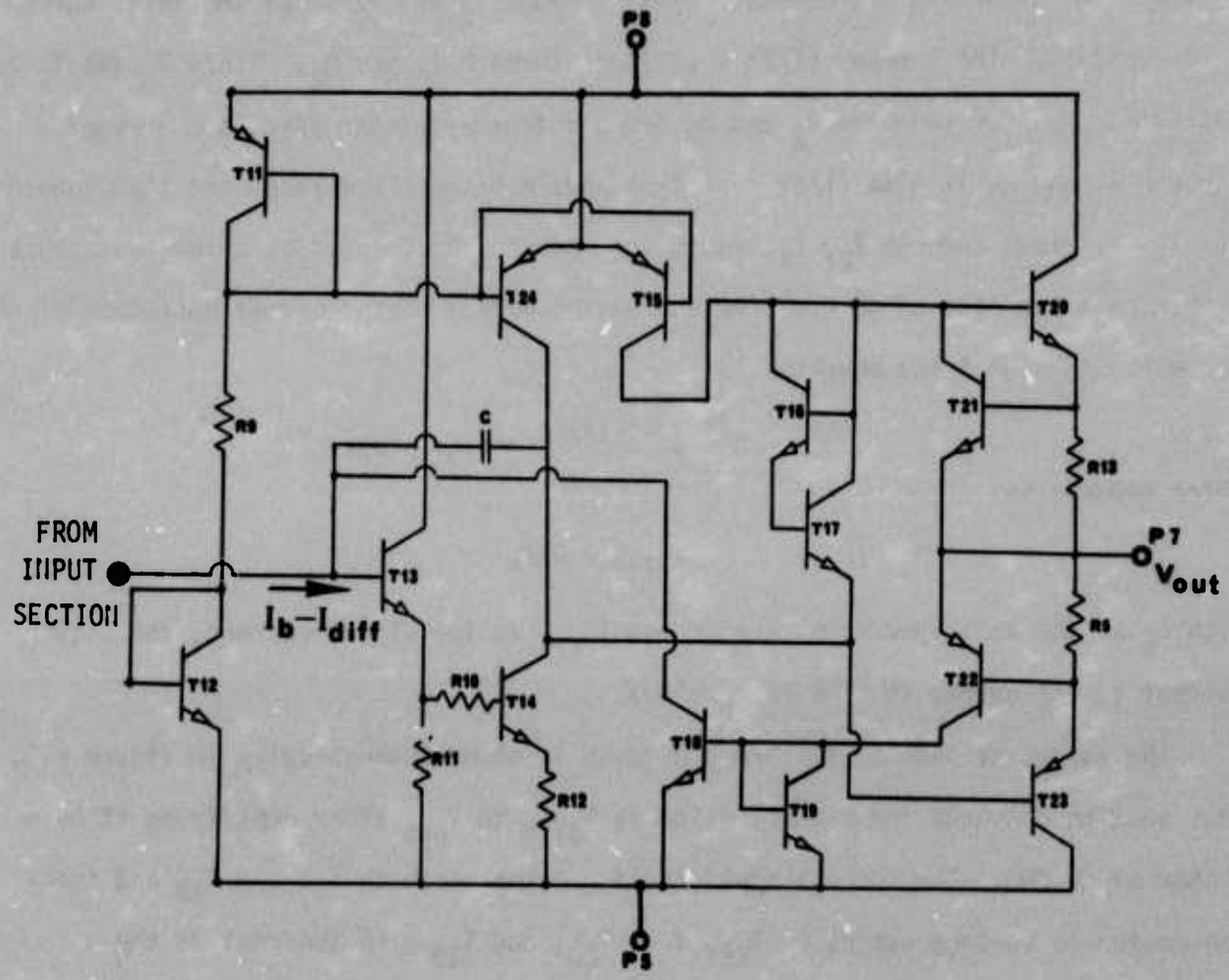

FIGURE B-3 OUTPUT SECTION OF 741 SCHEMATIC

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